

10 

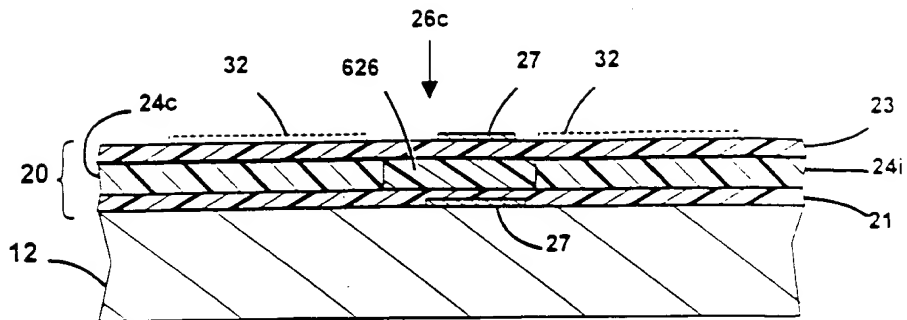


FIG.\_2

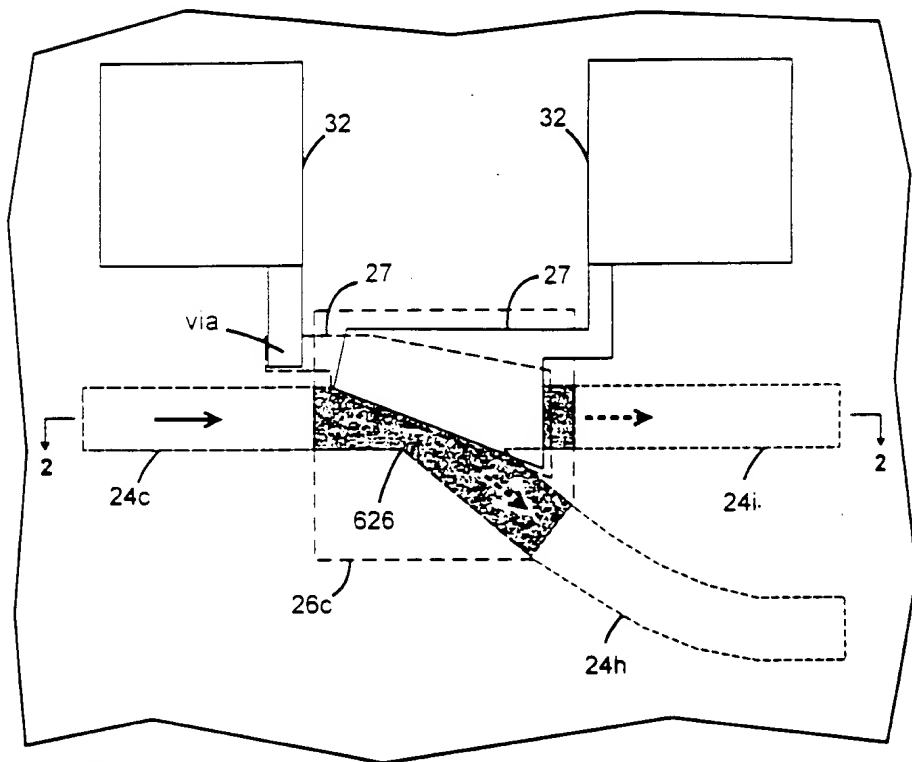


FIG.\_3

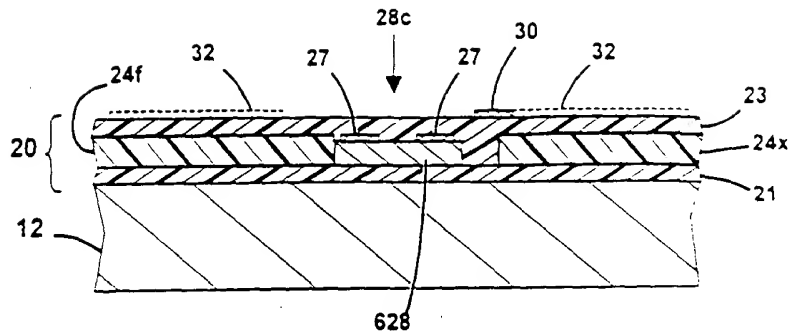
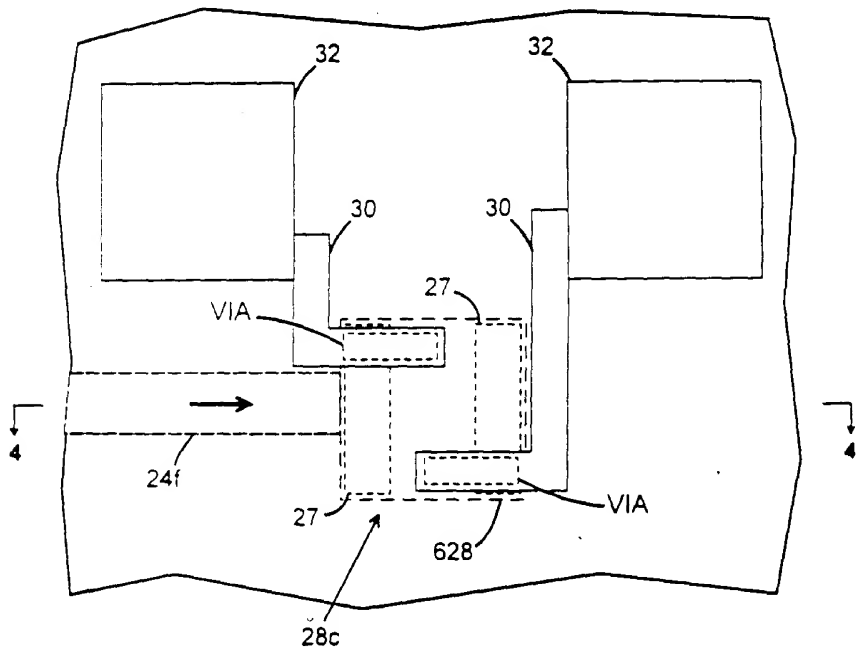
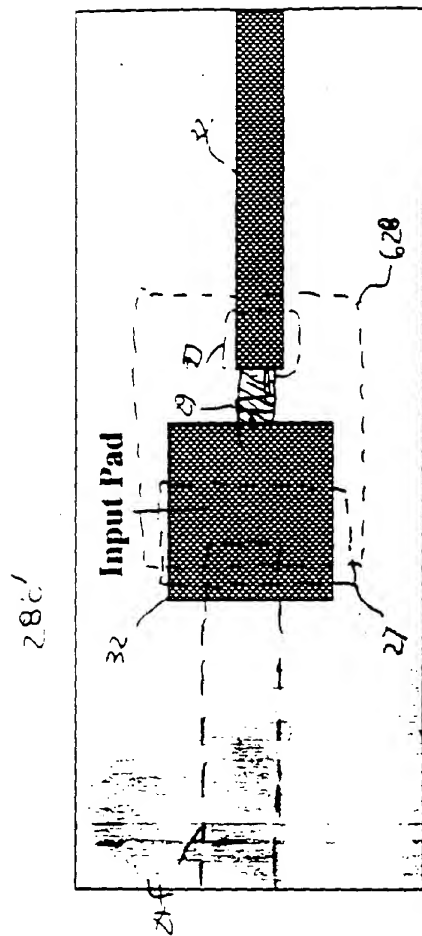


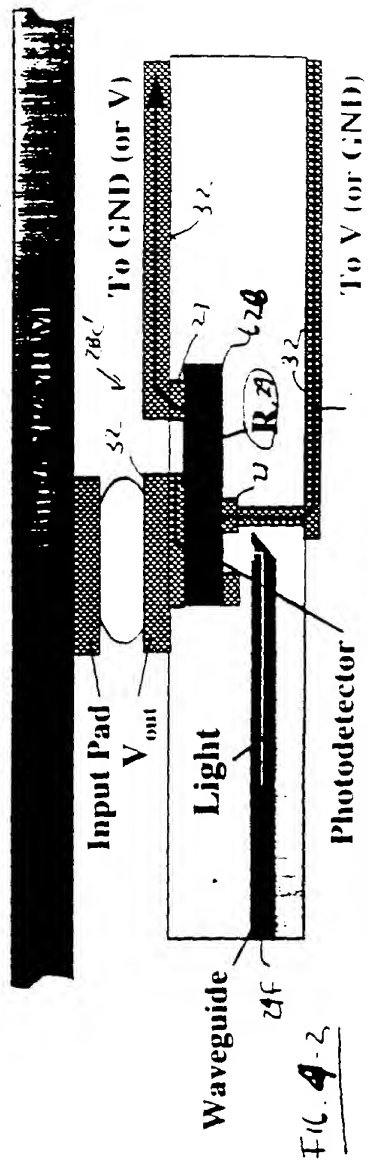
FIG. 4-1



**FIG. 5-1**



F16.5-2



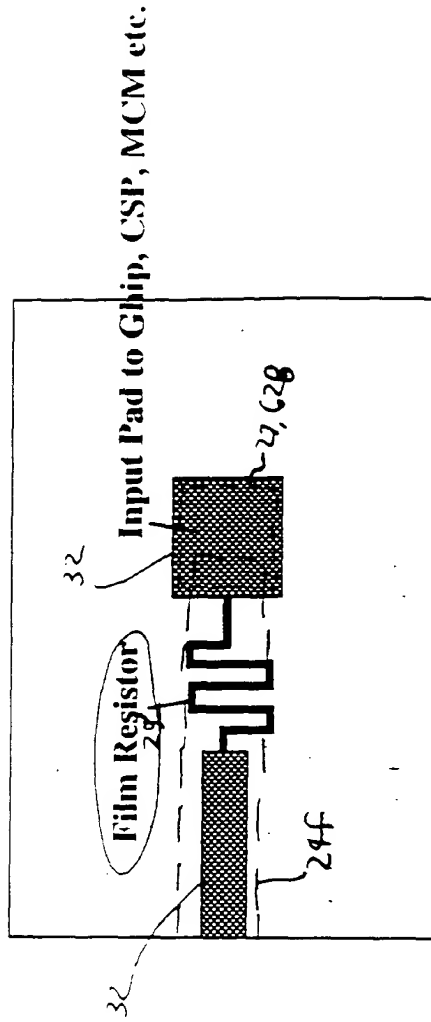


Fig. 5-3

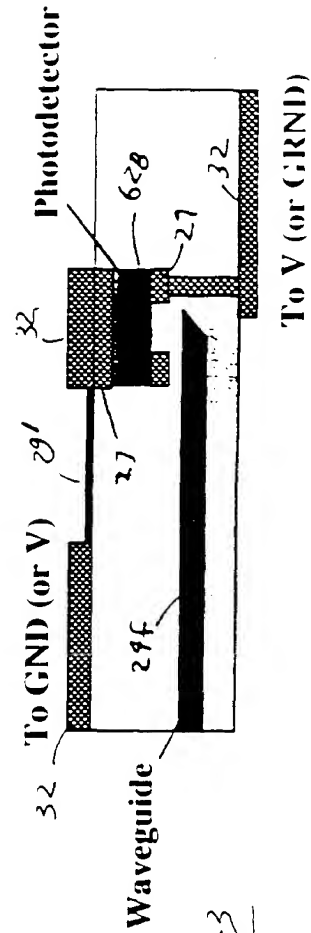
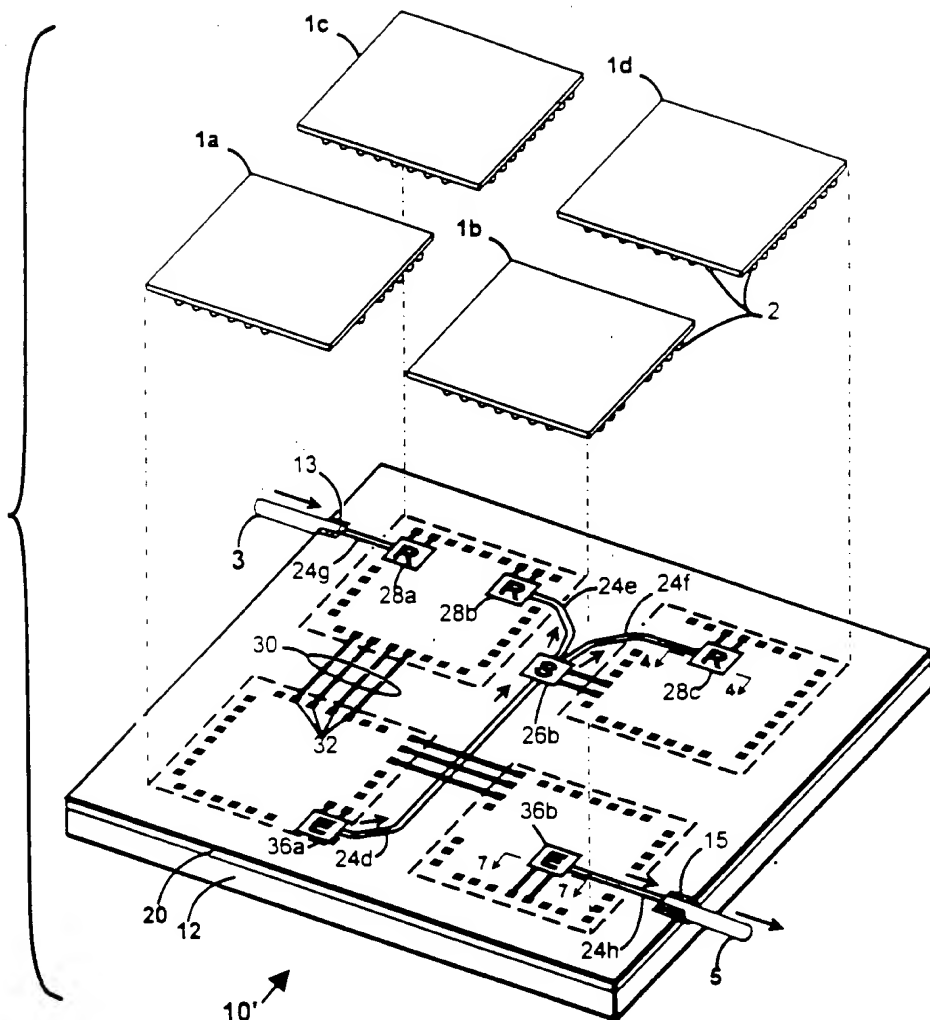
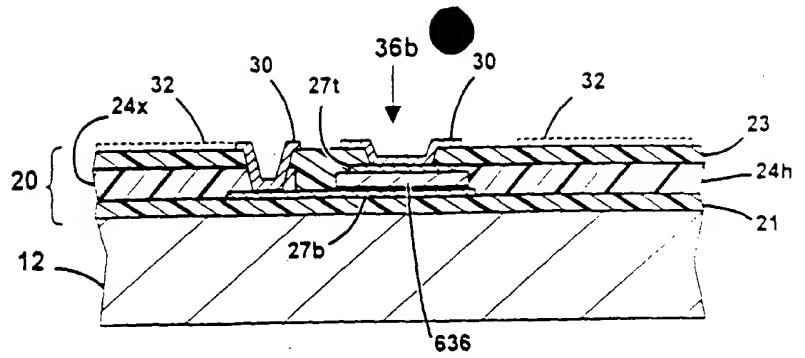


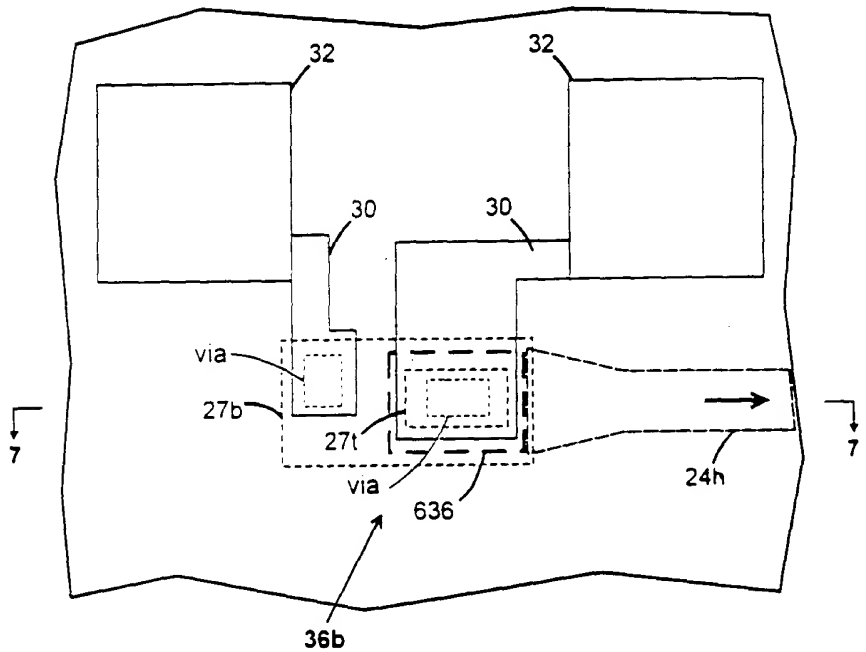
Fig. 4-3

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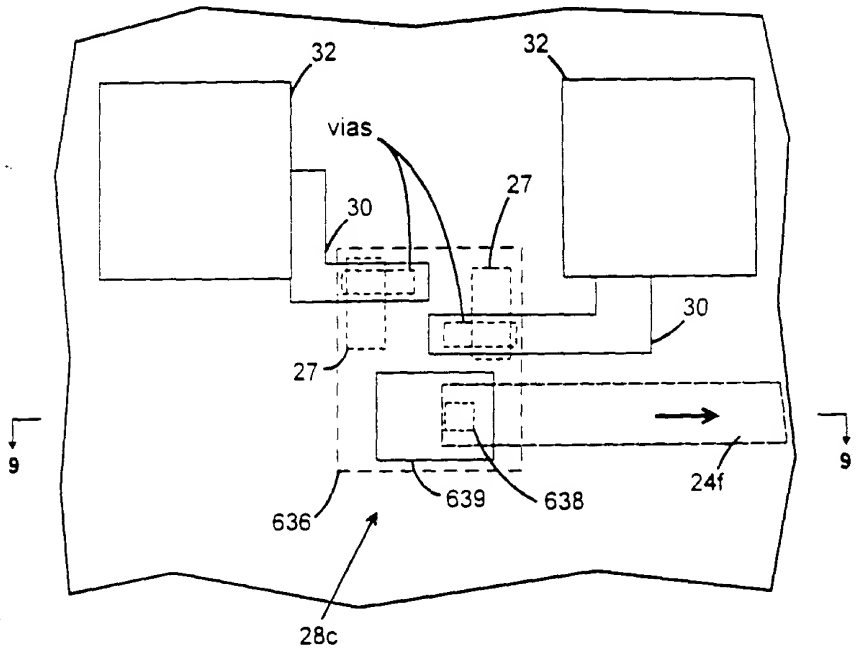
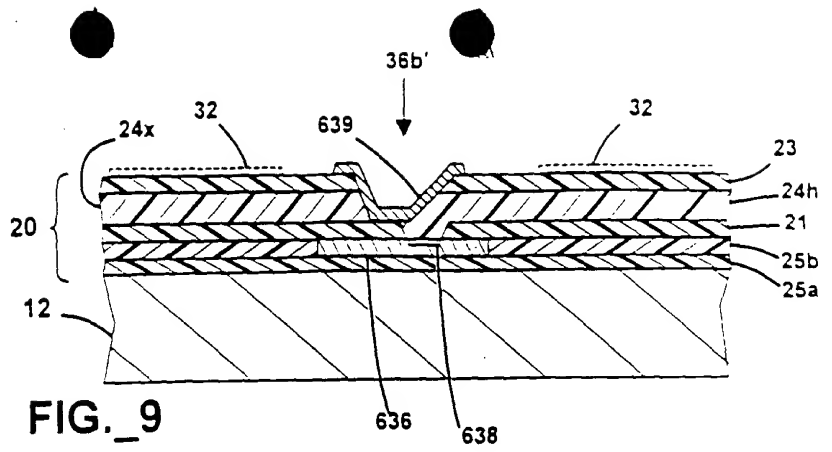




**FIG. 7**



**FIG. 8**



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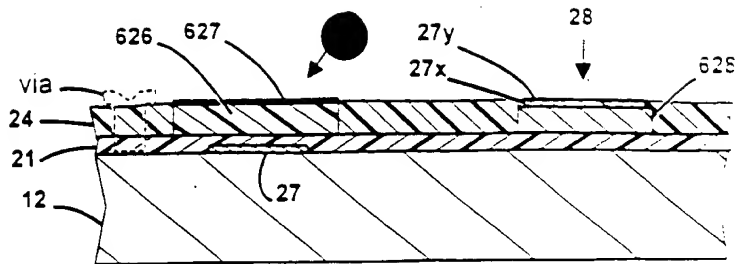


FIG. 15

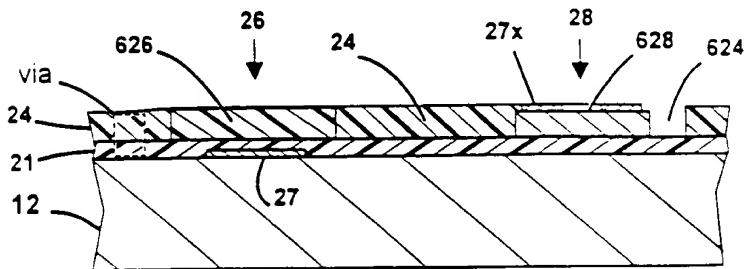


FIG. 16

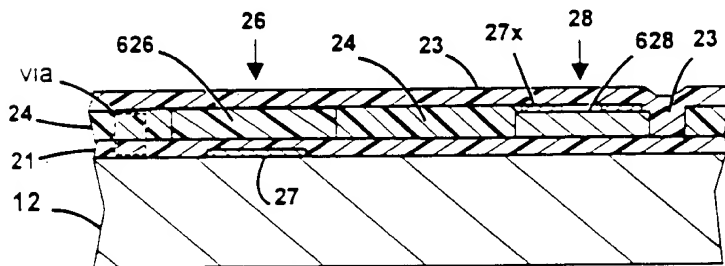


FIG. 17

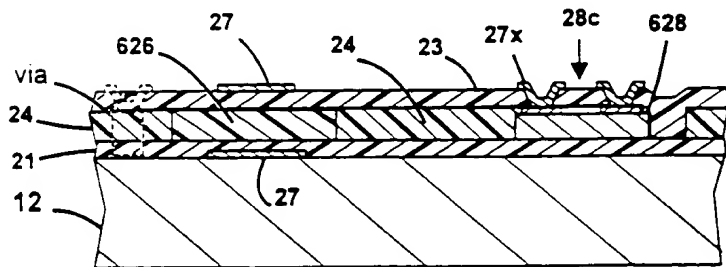


FIG. 18

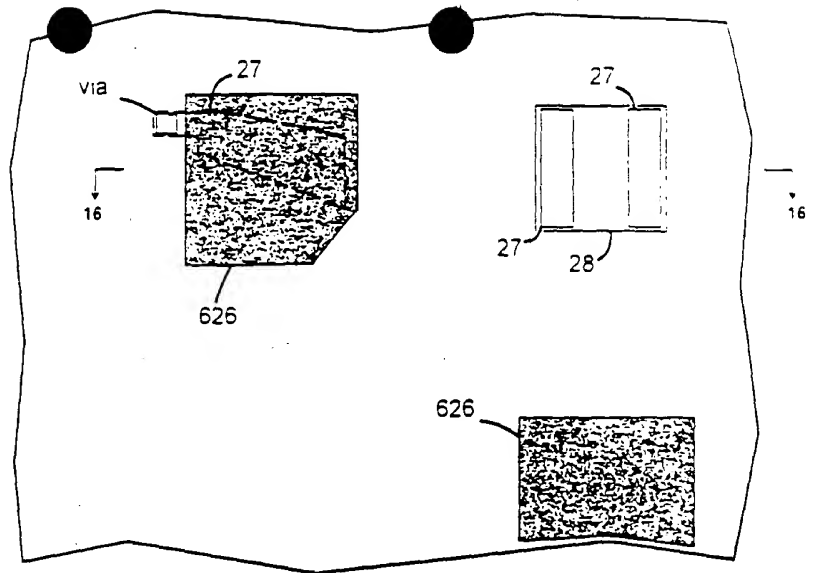


FIG.\_19

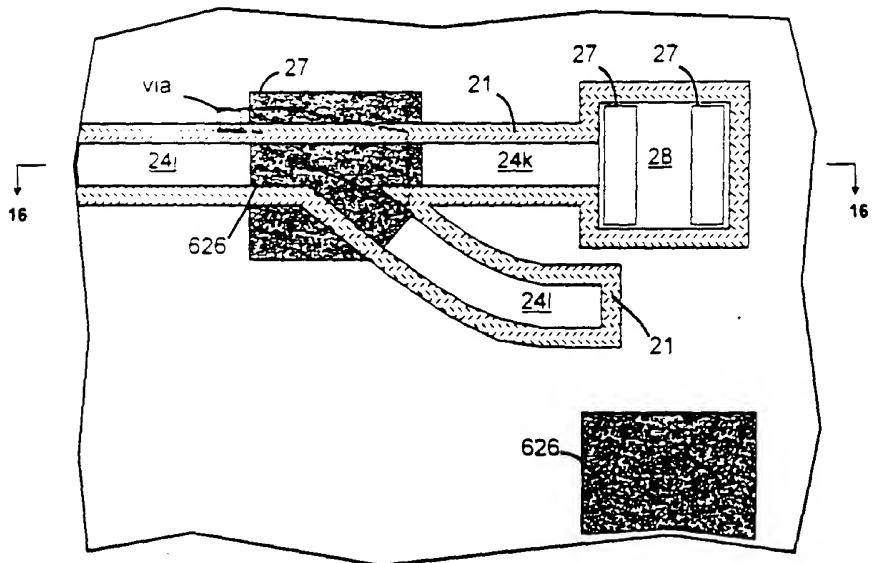
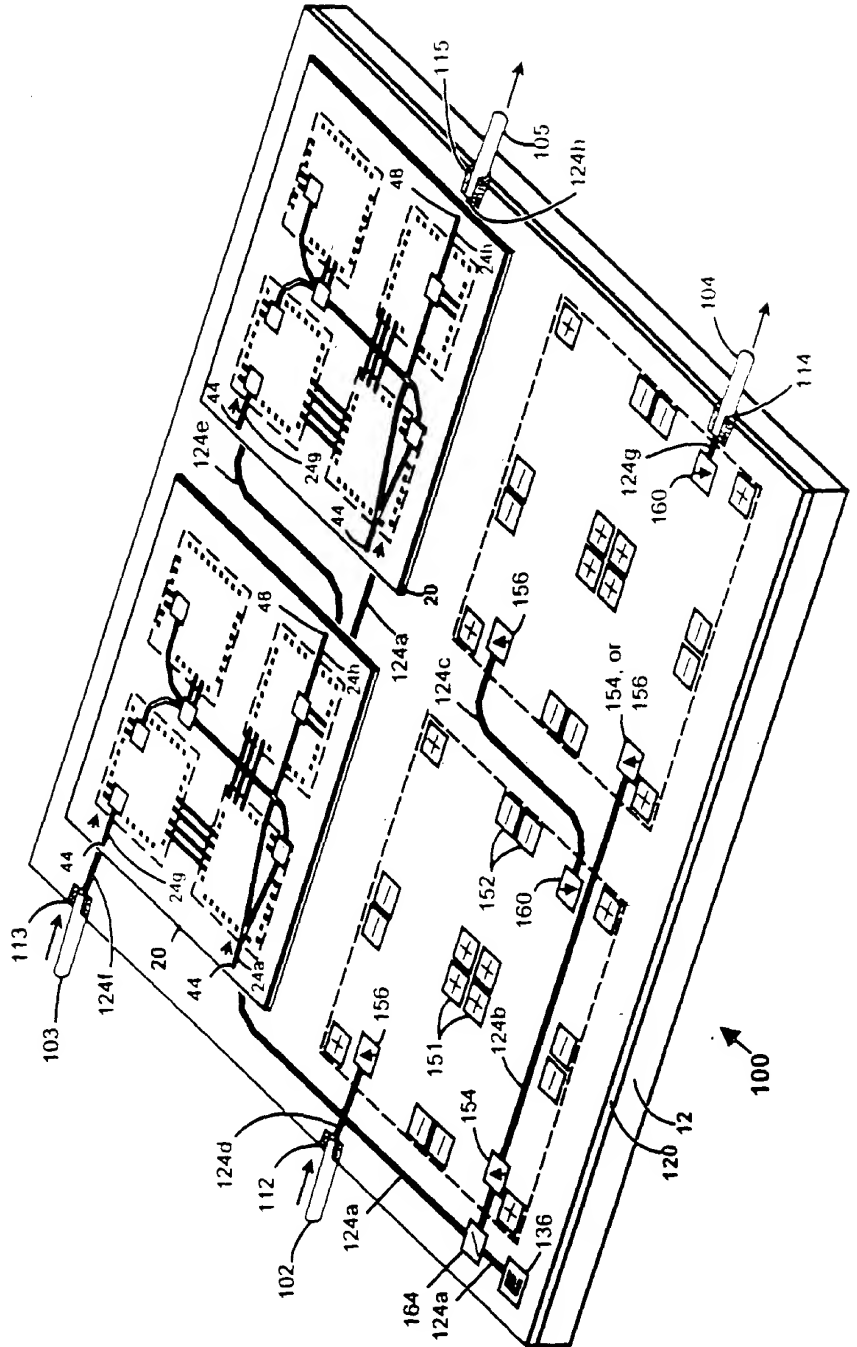


FIG.\_20



**FIG. 21**

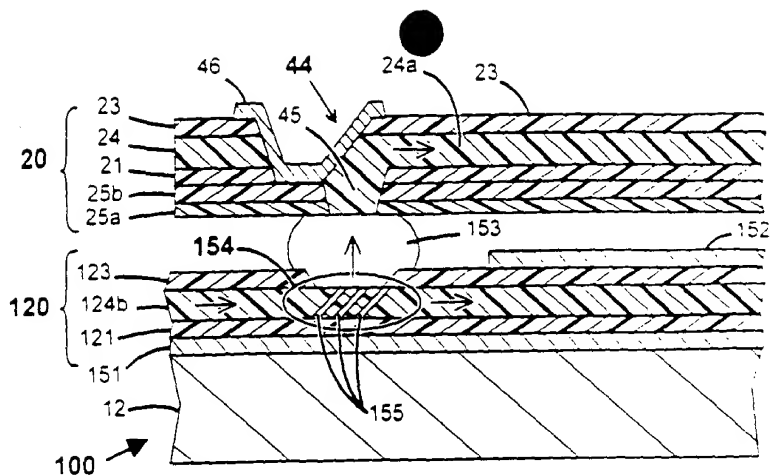


FIG. 22

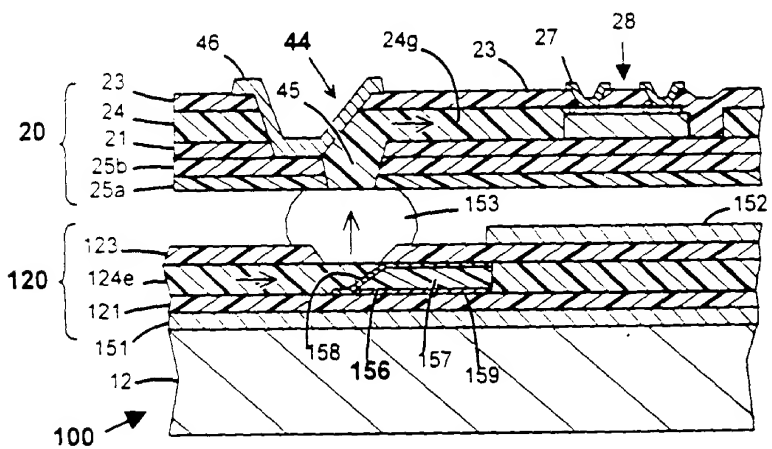


FIG. 23

102210-28529760

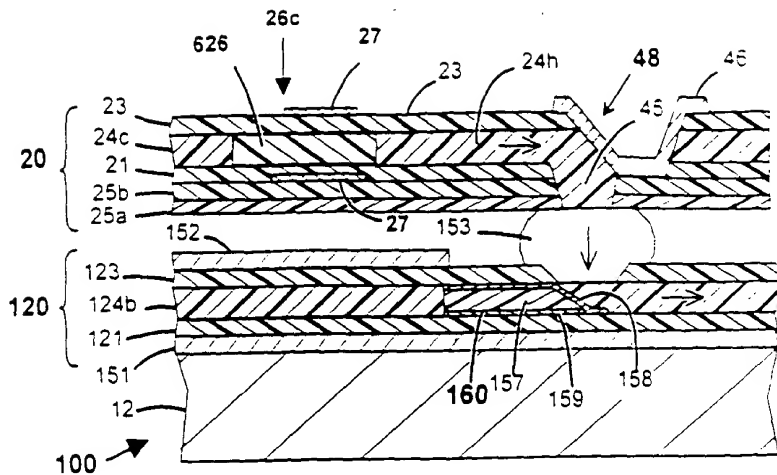


FIG. 24

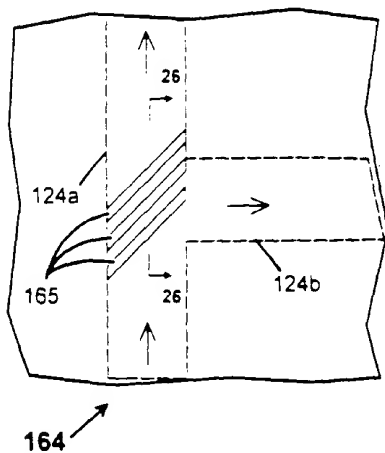


FIG. 25

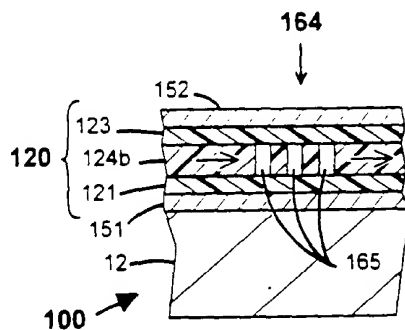


FIG. 26

102210-28529260

FIG.\_27

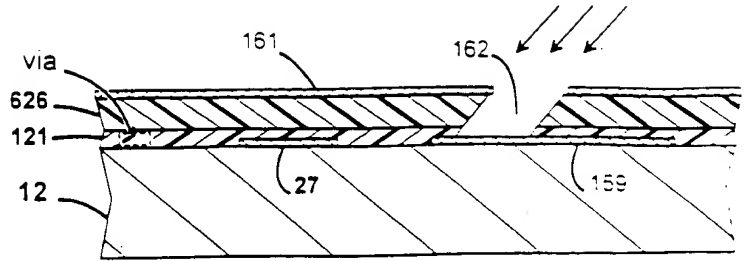


FIG.\_28

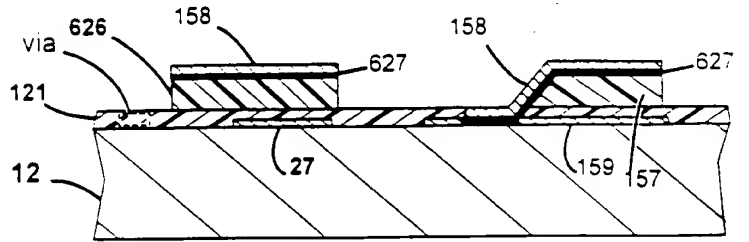


FIG.\_29

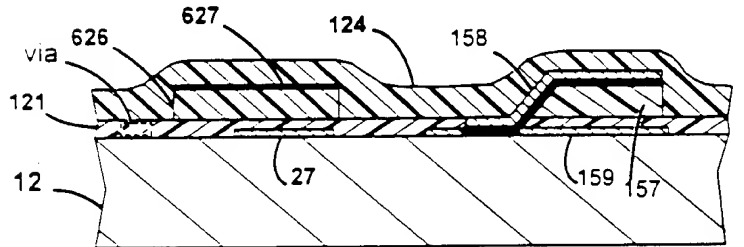
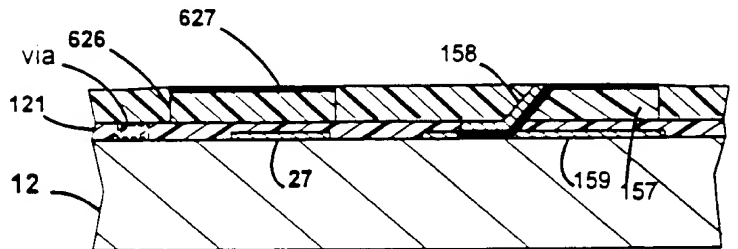
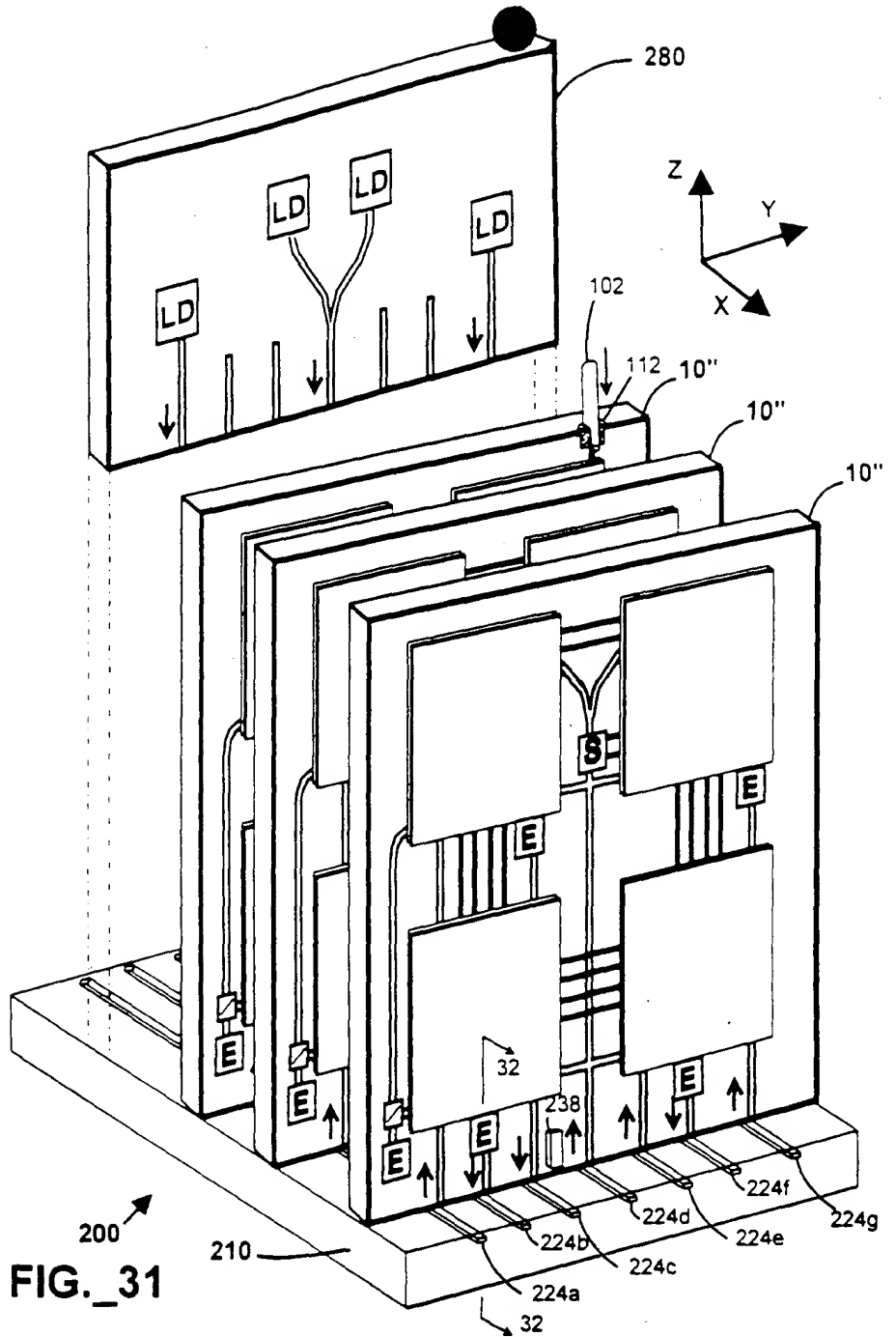


FIG.\_30

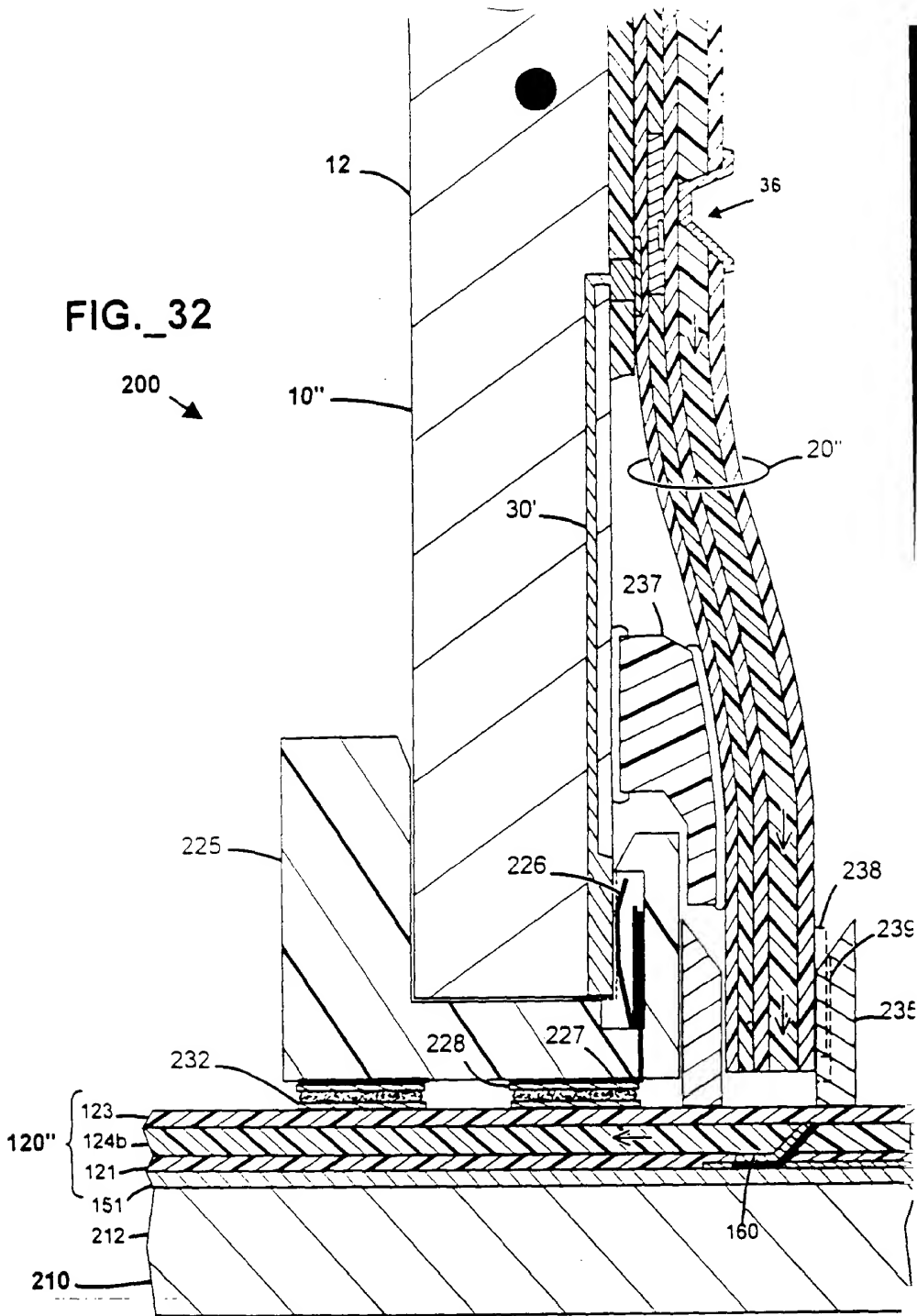






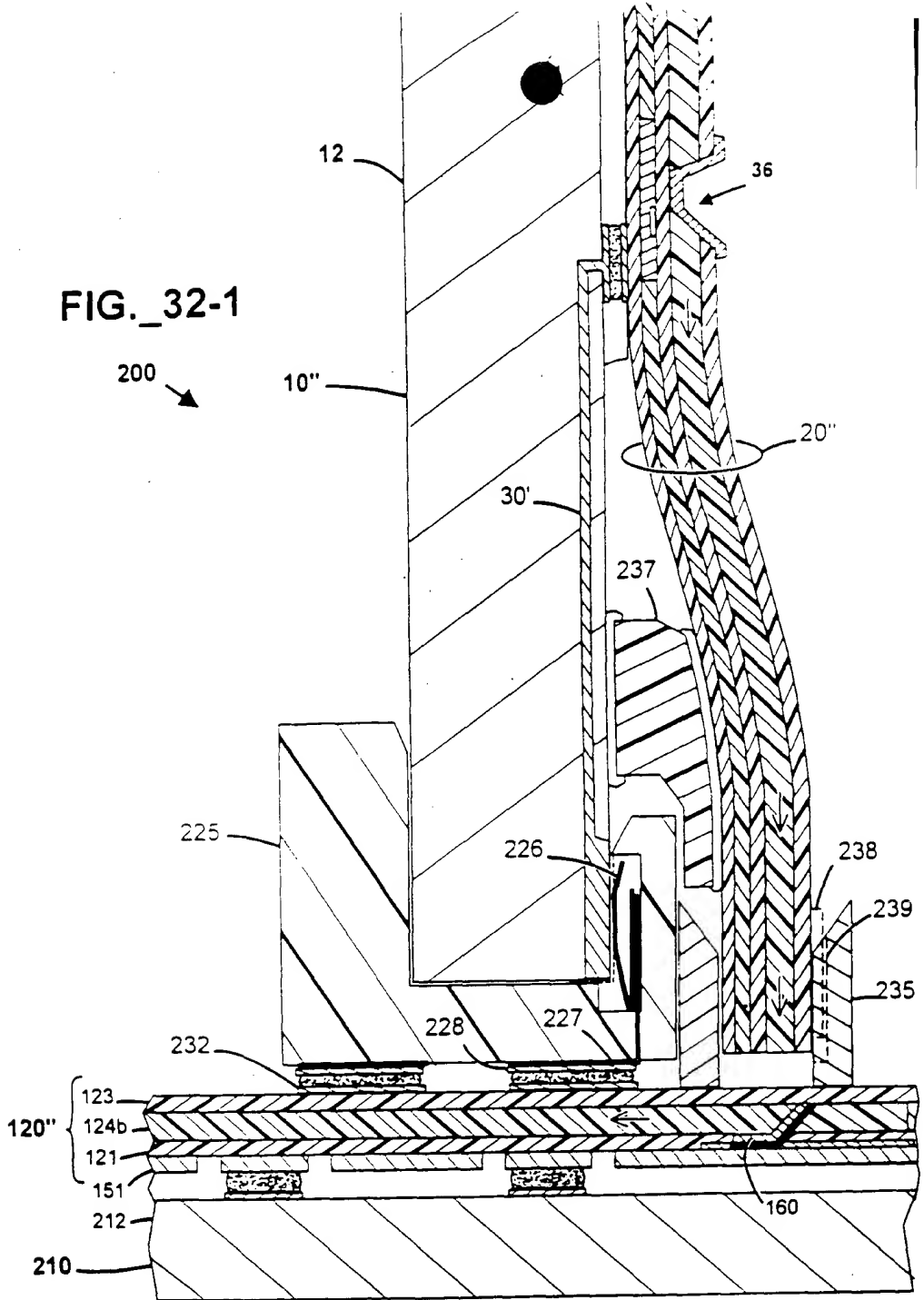
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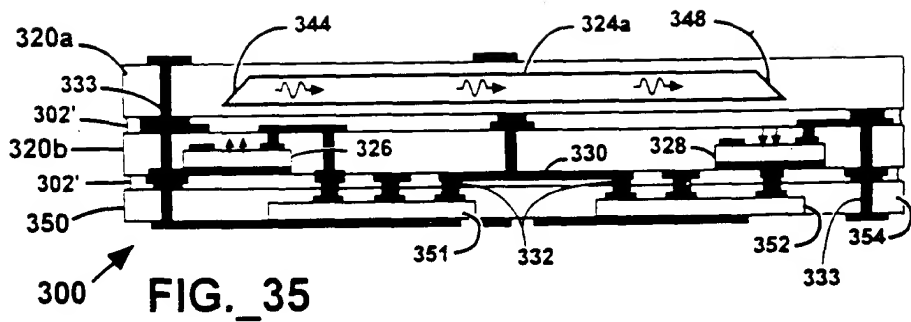
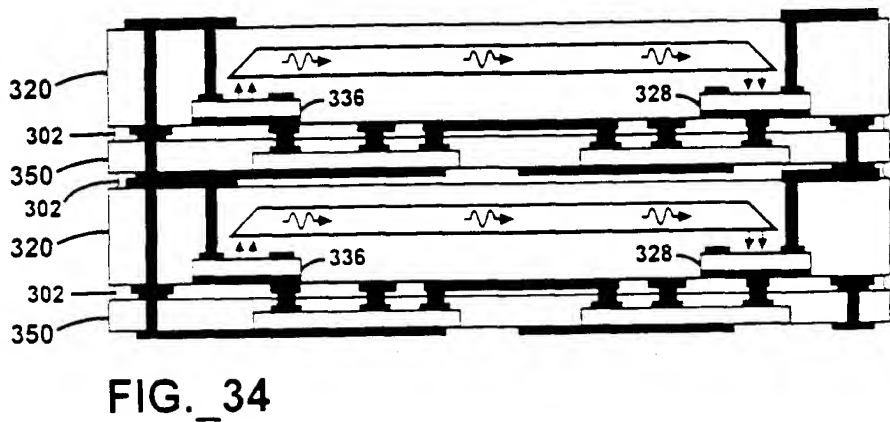
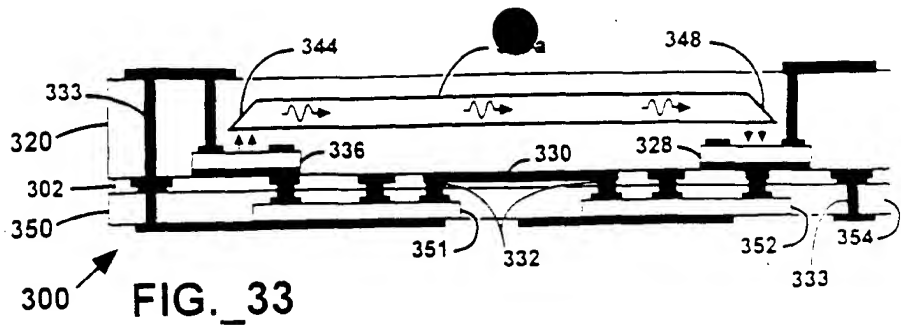
FIG.\_32



09767582.012201

FIG. 32-1





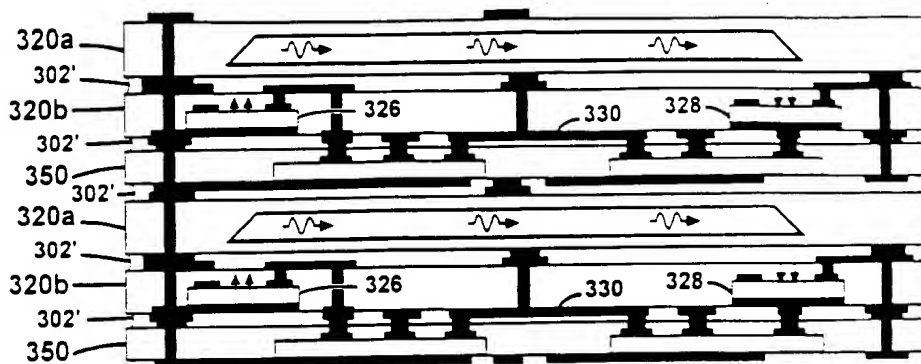
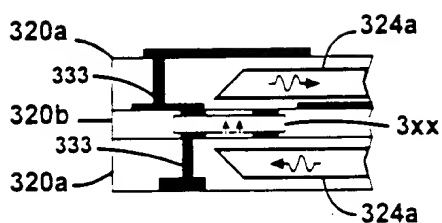
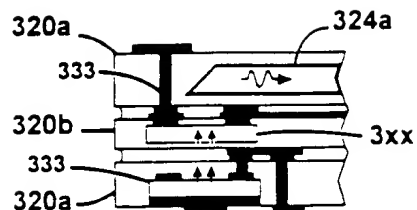


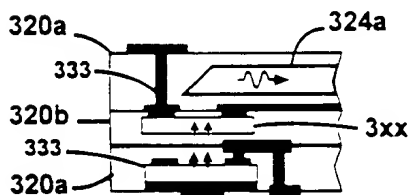
FIG. 36



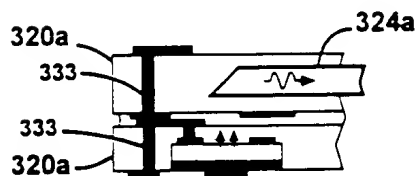
**FIG. 37-1**



**FIG. 37-2**



**FIG. 37-3**



**FIG. 37-4**

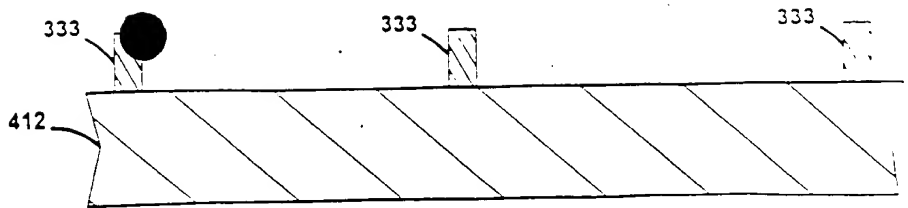


FIG.\_38

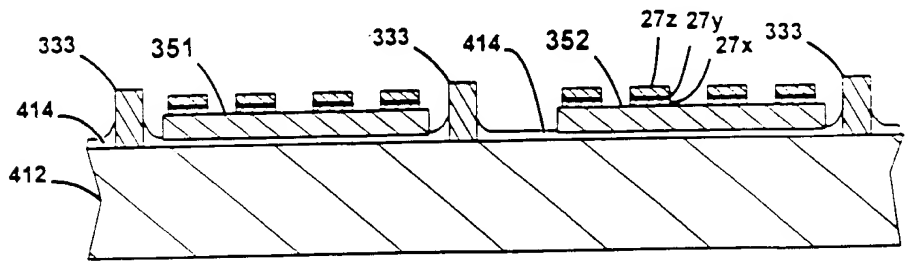


FIG.\_39

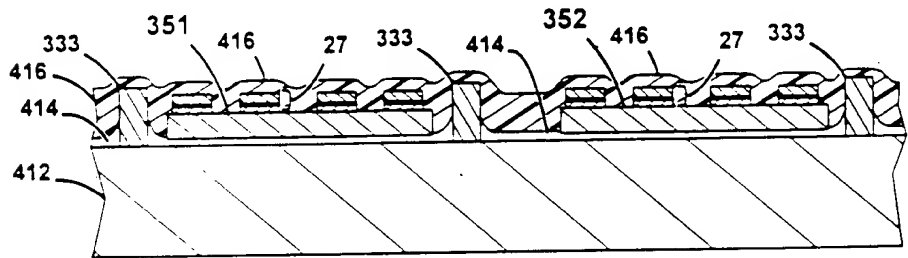


FIG.\_40

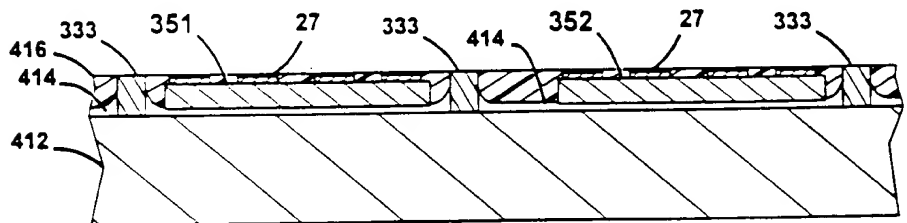


FIG.\_41

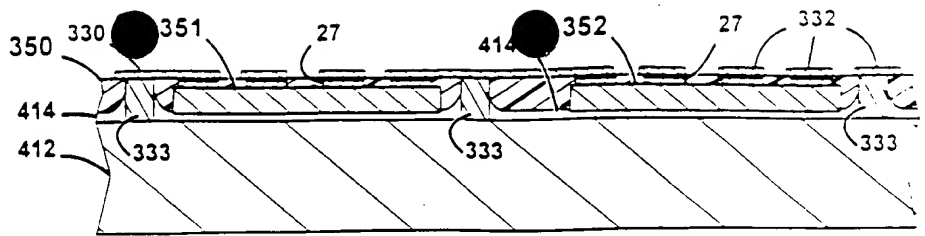


FIG. 42

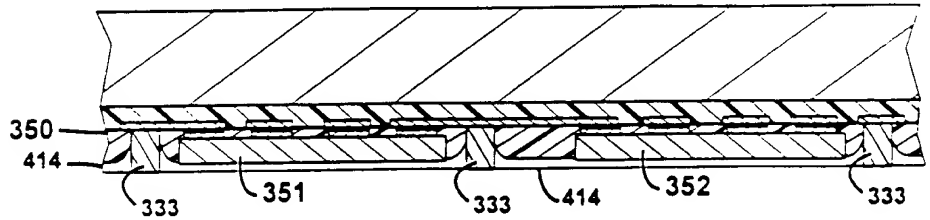


FIG. 43

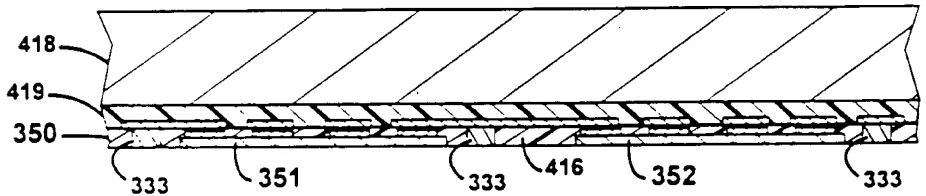


FIG. 44

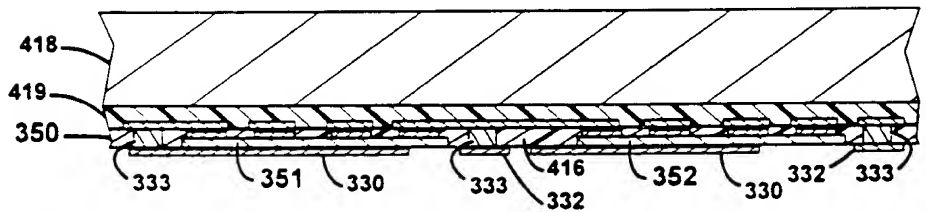
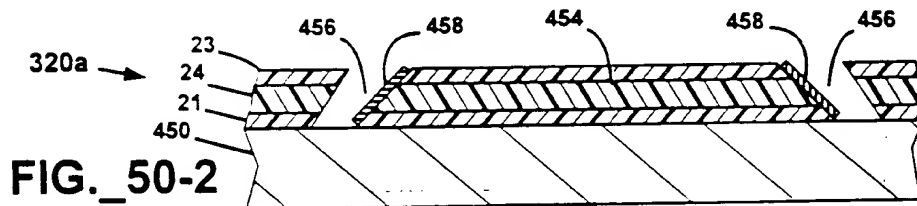
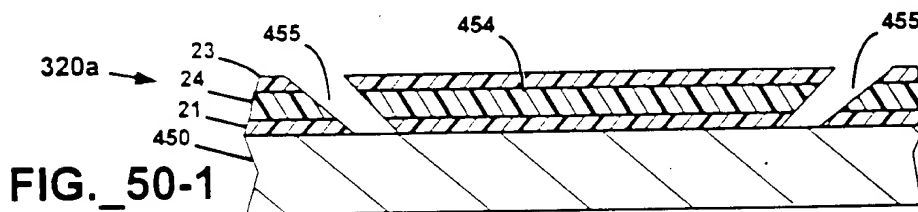
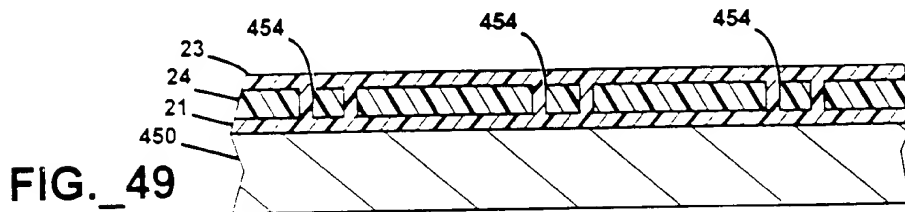
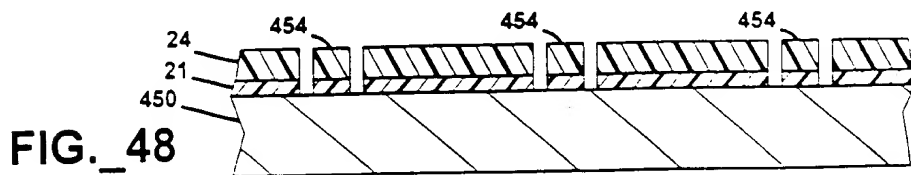
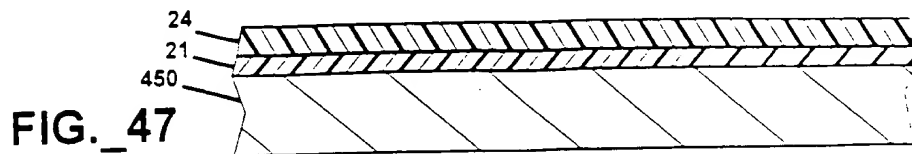
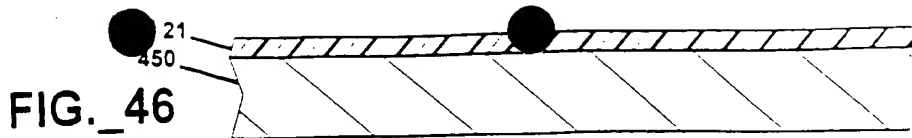


FIG. 45



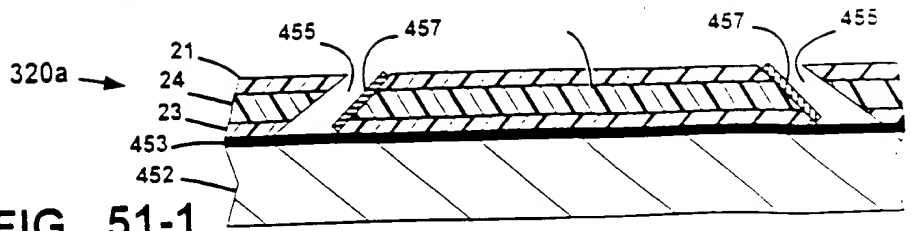


FIG. 51-1

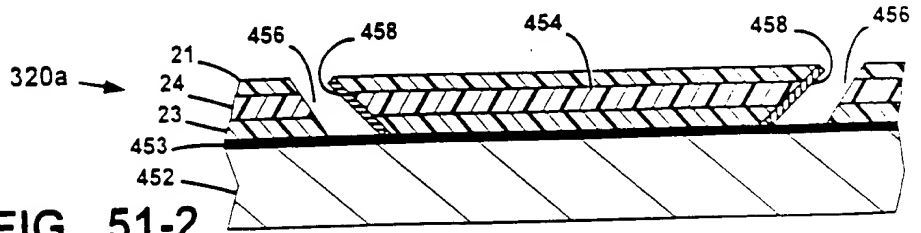


FIG. 51-2

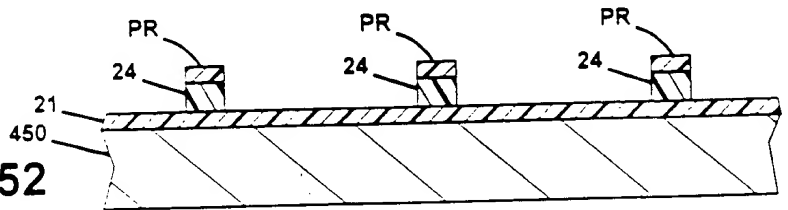


FIG. 52

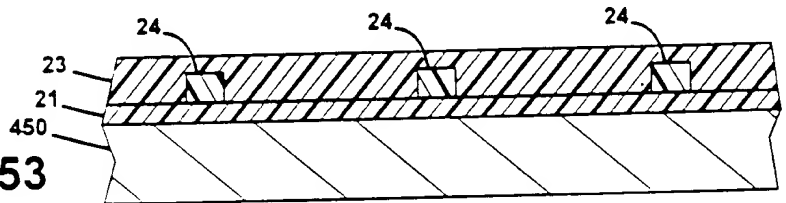
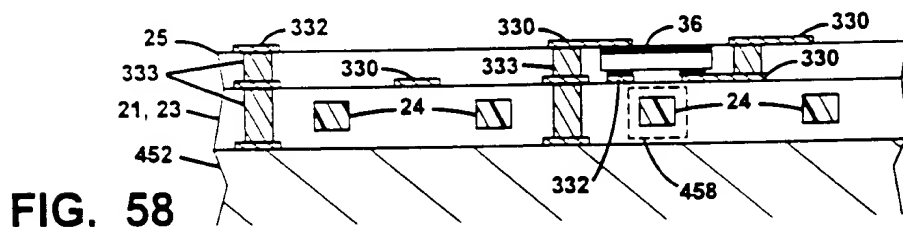
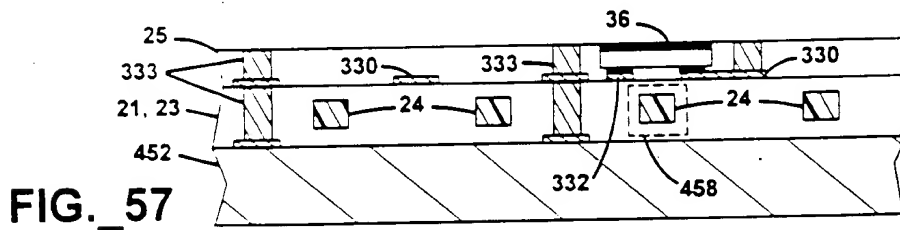
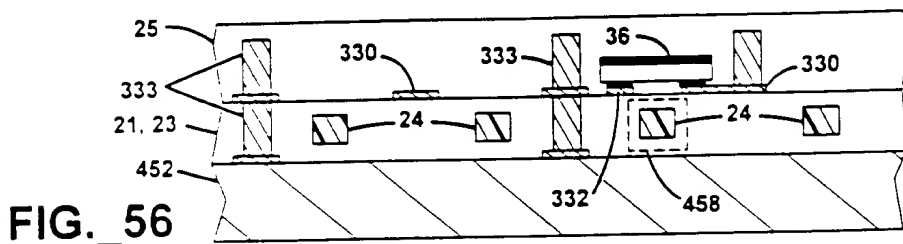
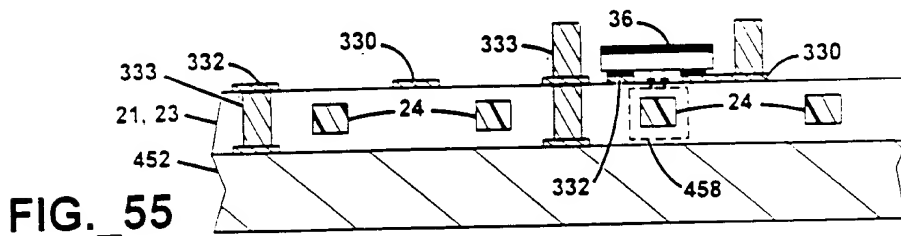
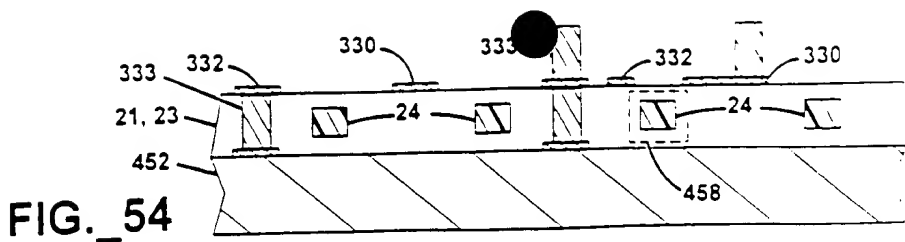


FIG. 53





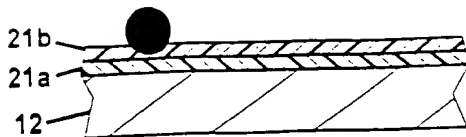


FIG.\_59

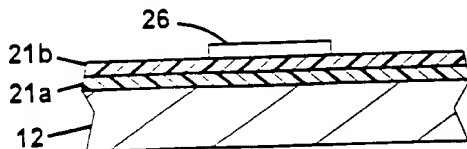


FIG.\_60

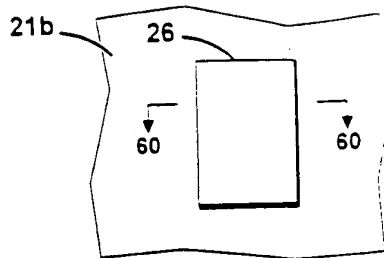


FIG.\_61

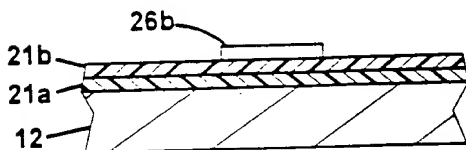


FIG.\_62

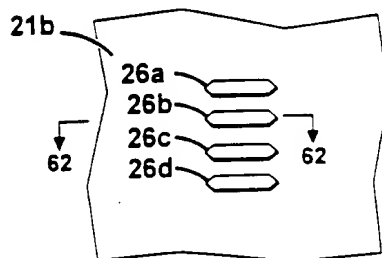


FIG.\_63

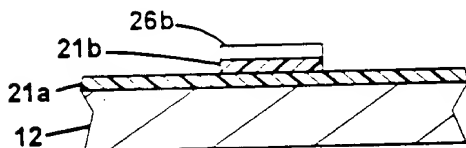


FIG.\_64

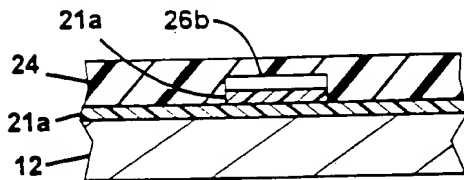


FIG.\_65

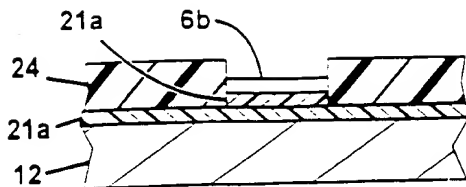


FIG. 66

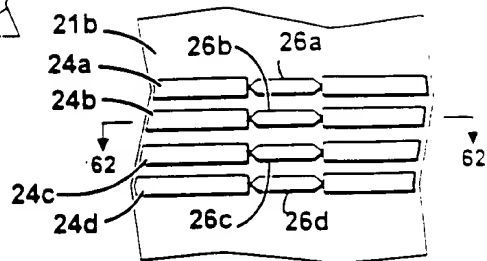


FIG. 67

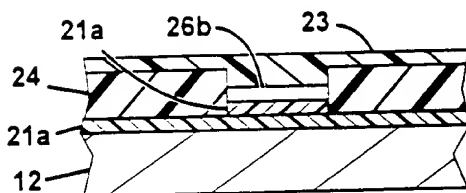


FIG. 68

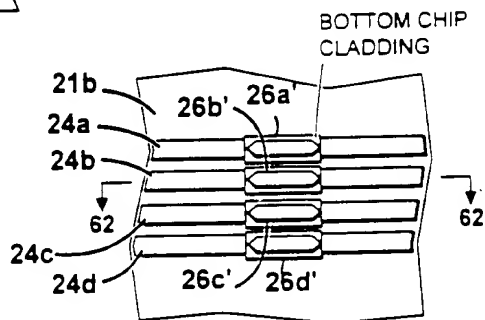
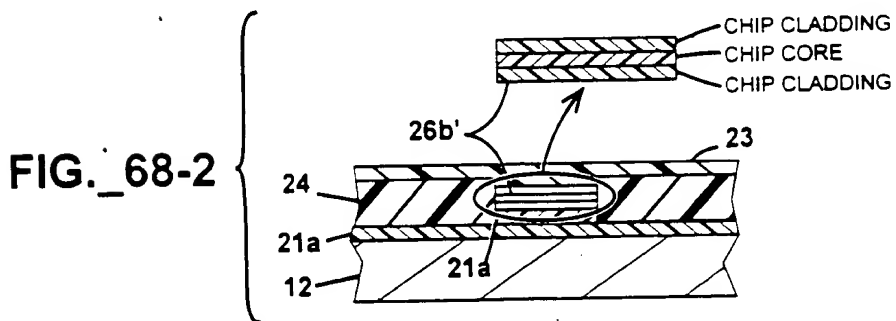


FIG. 67-2



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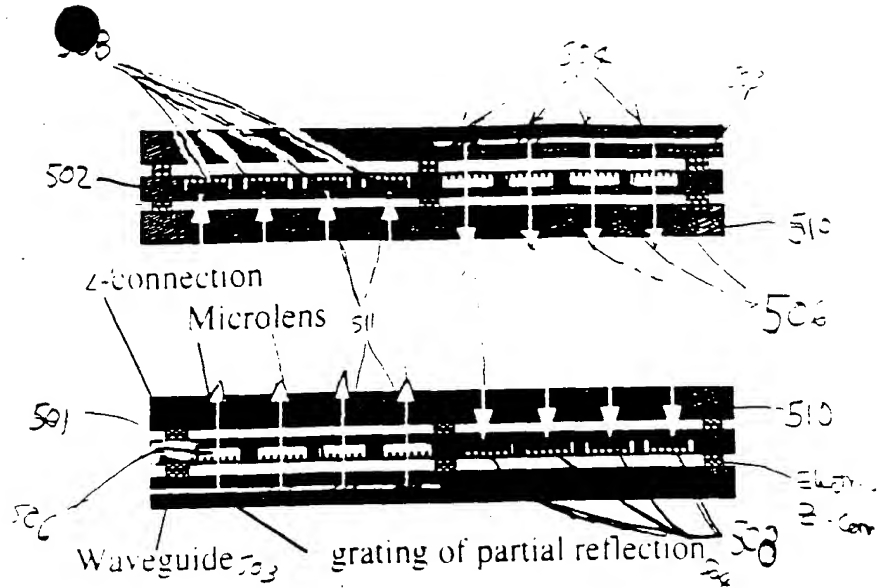


FIG. 69

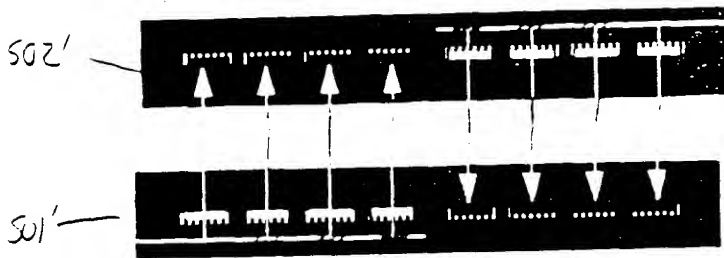
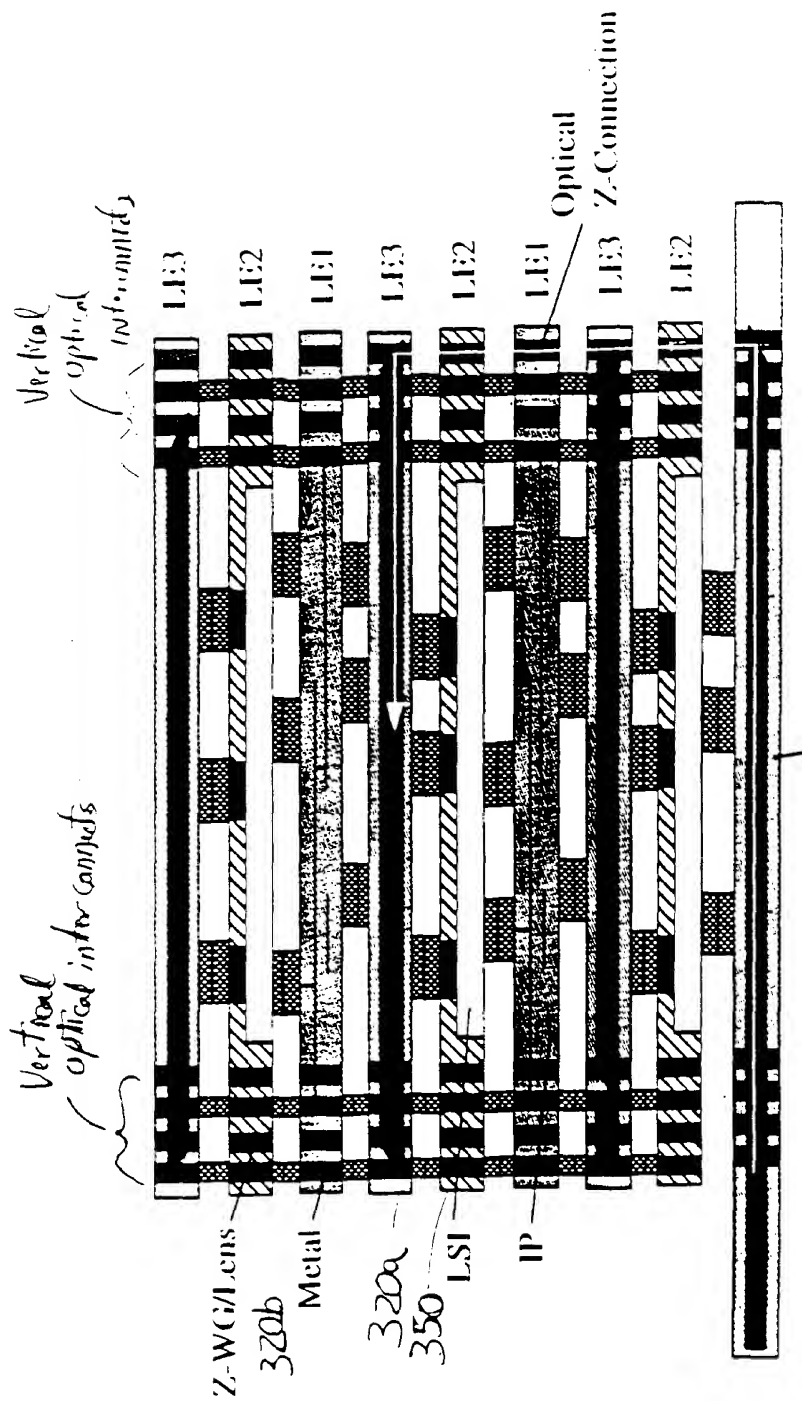
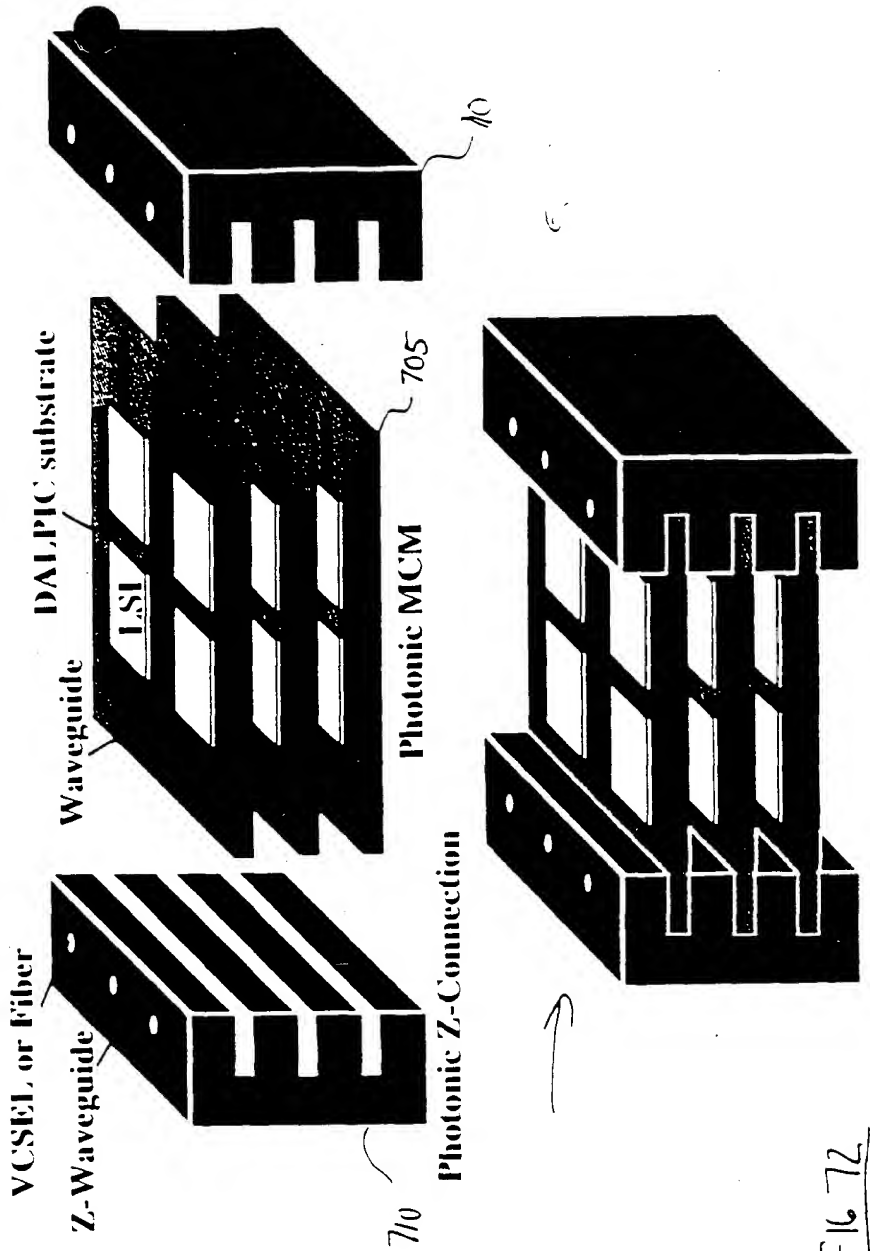


FIG. 70

**THE**  
**NEW**  
**YORK**  
**PUBLIC**  
**LIBRARY**  
**ASTOR**  
**TENNYSON**  
**AND**  
**TILDEN**

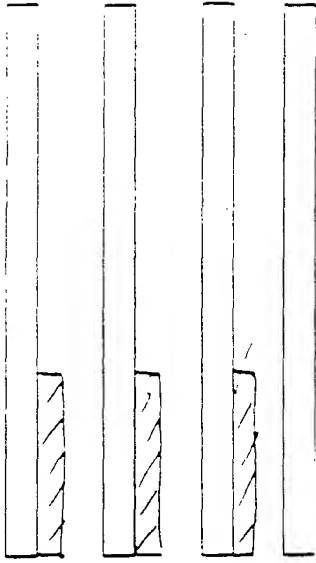
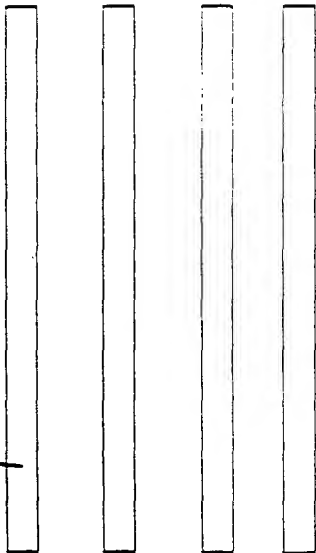


## Optical Backplane

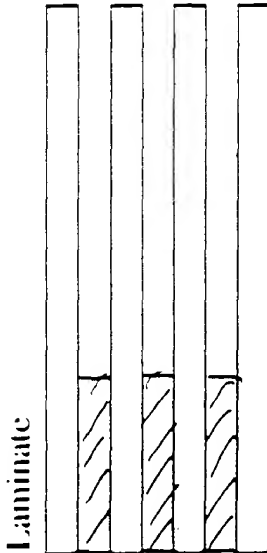


Flexible Photo-imageable sheet (Polyguide)

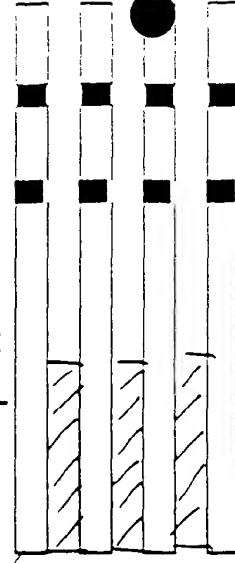
Bonding sheet attach



Laminate



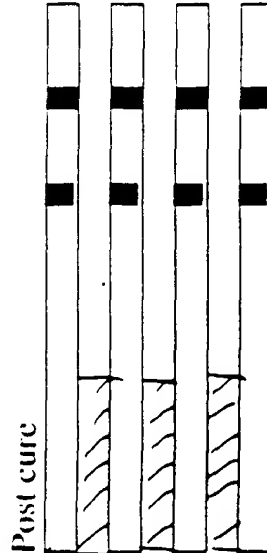
SOLNET process



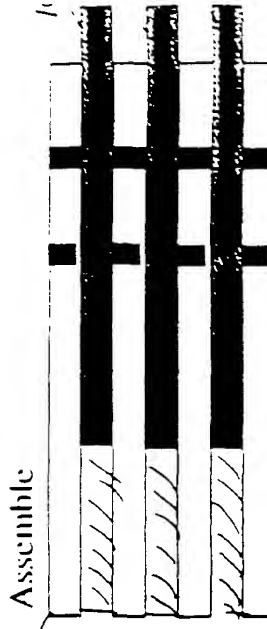
710



Post cure

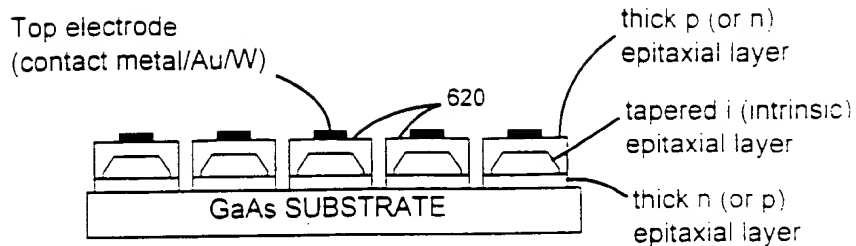


Assembly

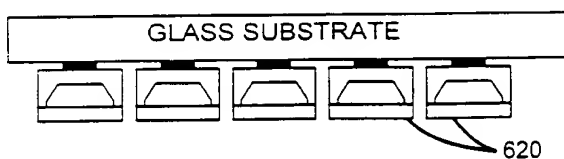


710

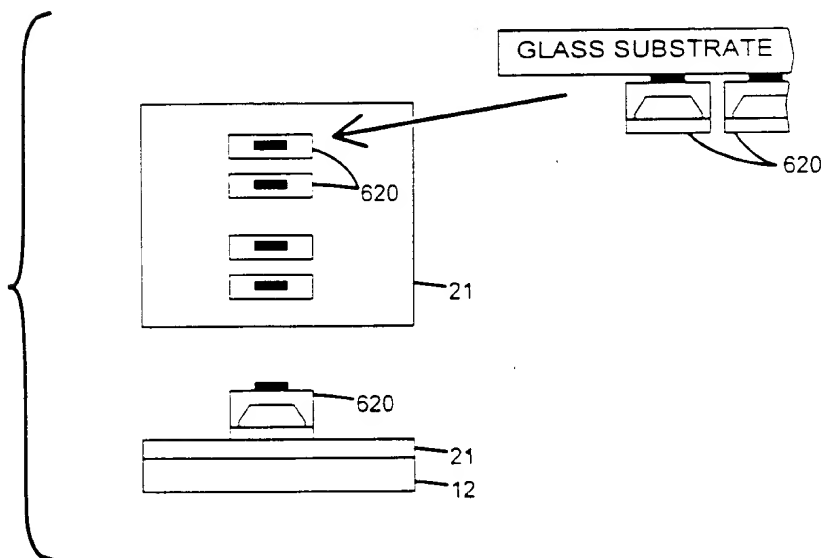
FIG. 73



**FIG.\_74** (Epitaxial growth and patterning)



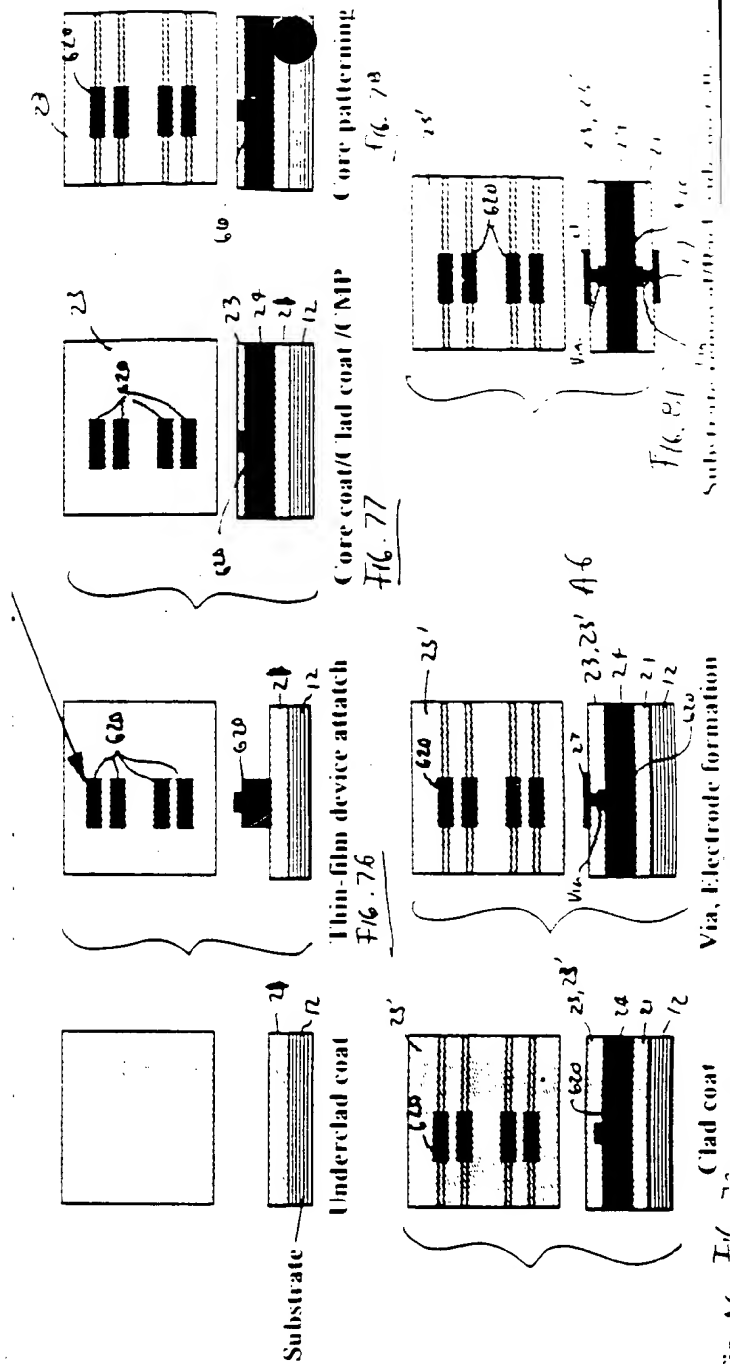
**FIG.\_75** (Epitaxial liftoff)

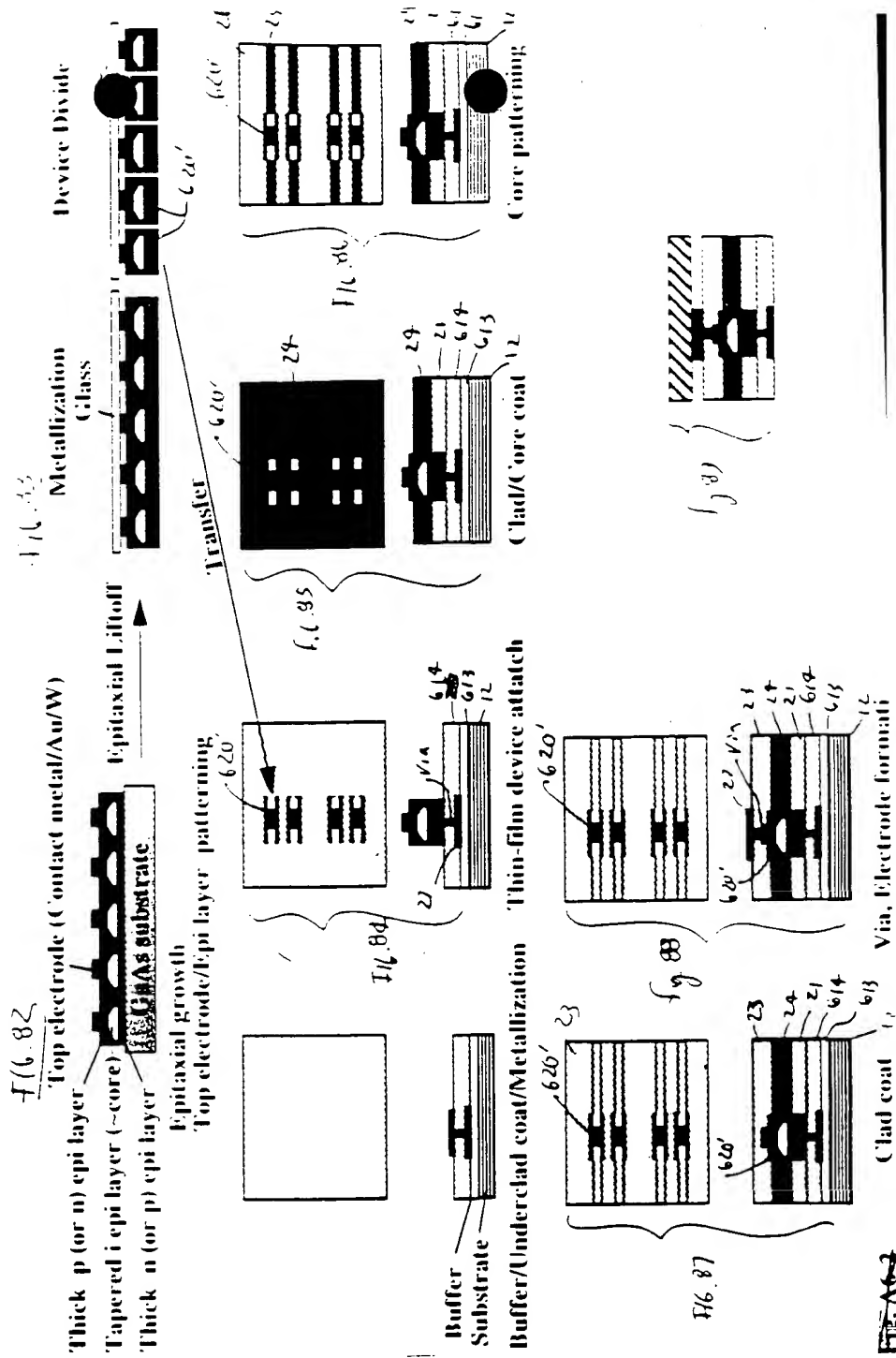


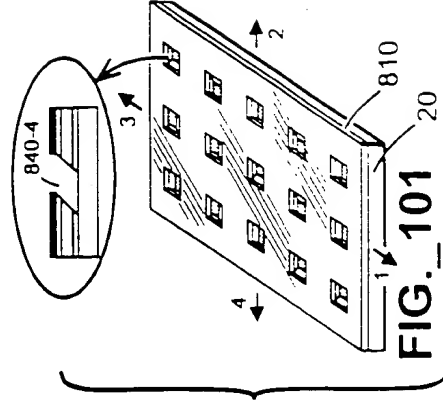
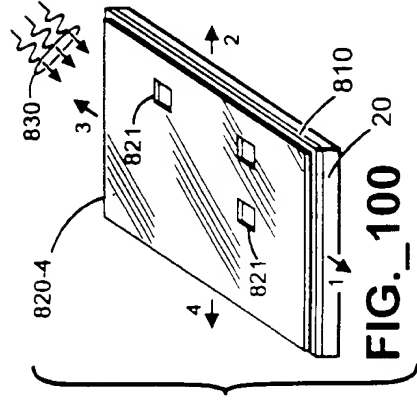
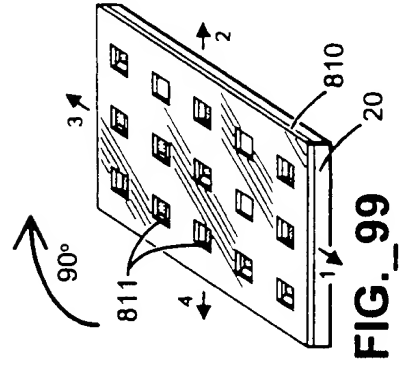
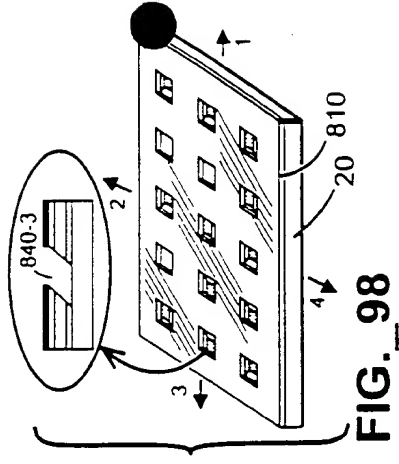
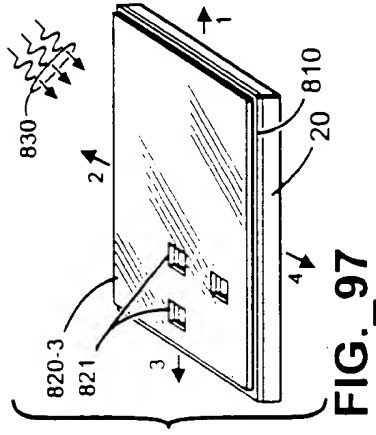
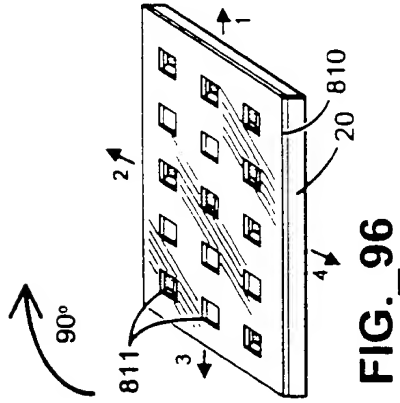
**FIG.\_76** (Transfer)

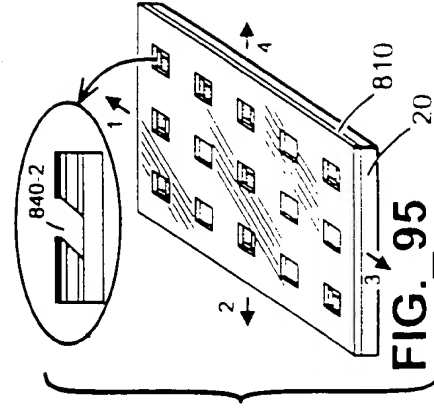
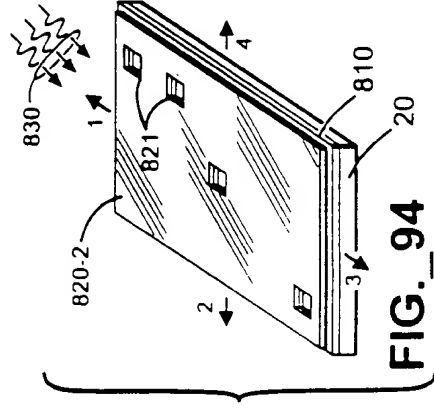
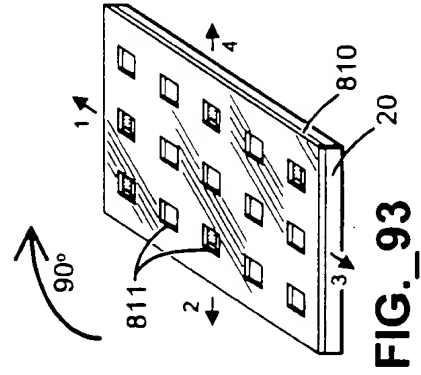
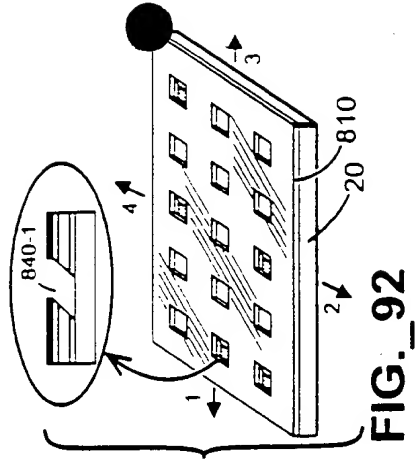
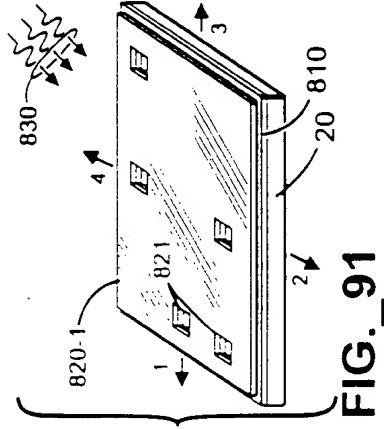
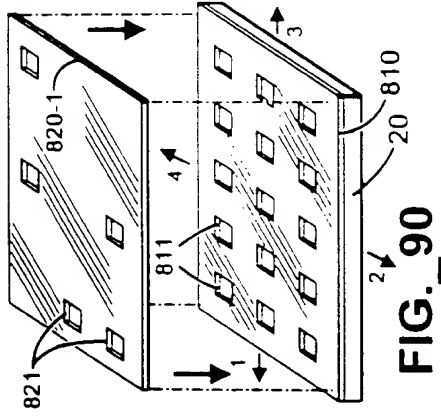
09767582.012201

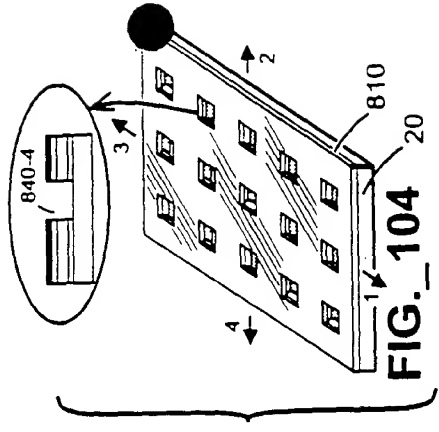
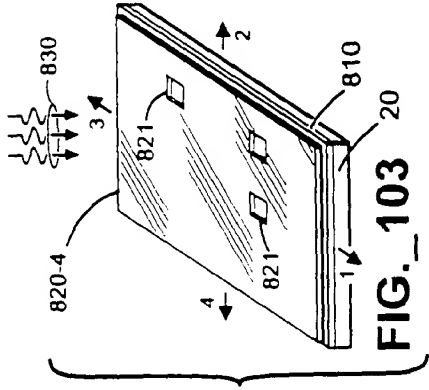
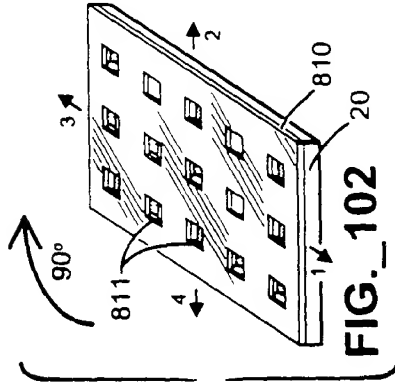












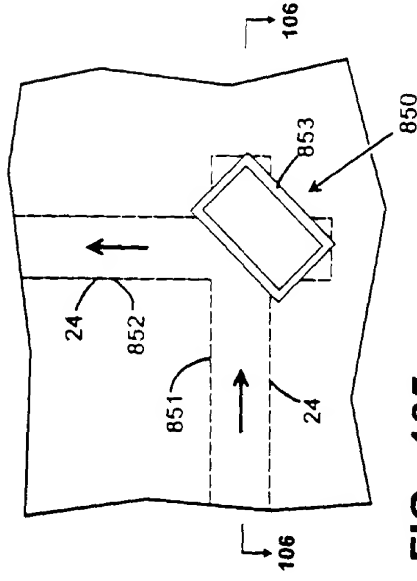


FIG. 105

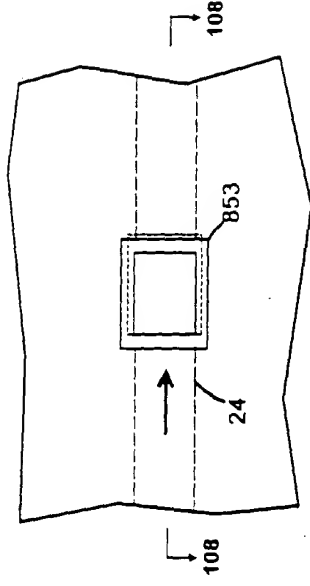


FIG. 107

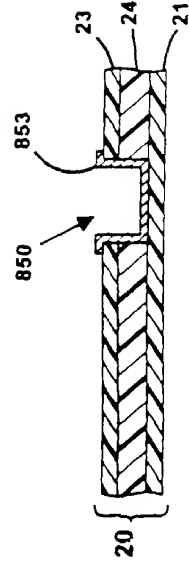


FIG. 106

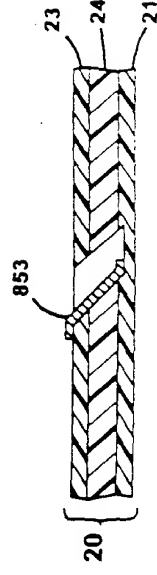


FIG. 108

GS CX/CXX OE Solution --- OE-3D-Stack

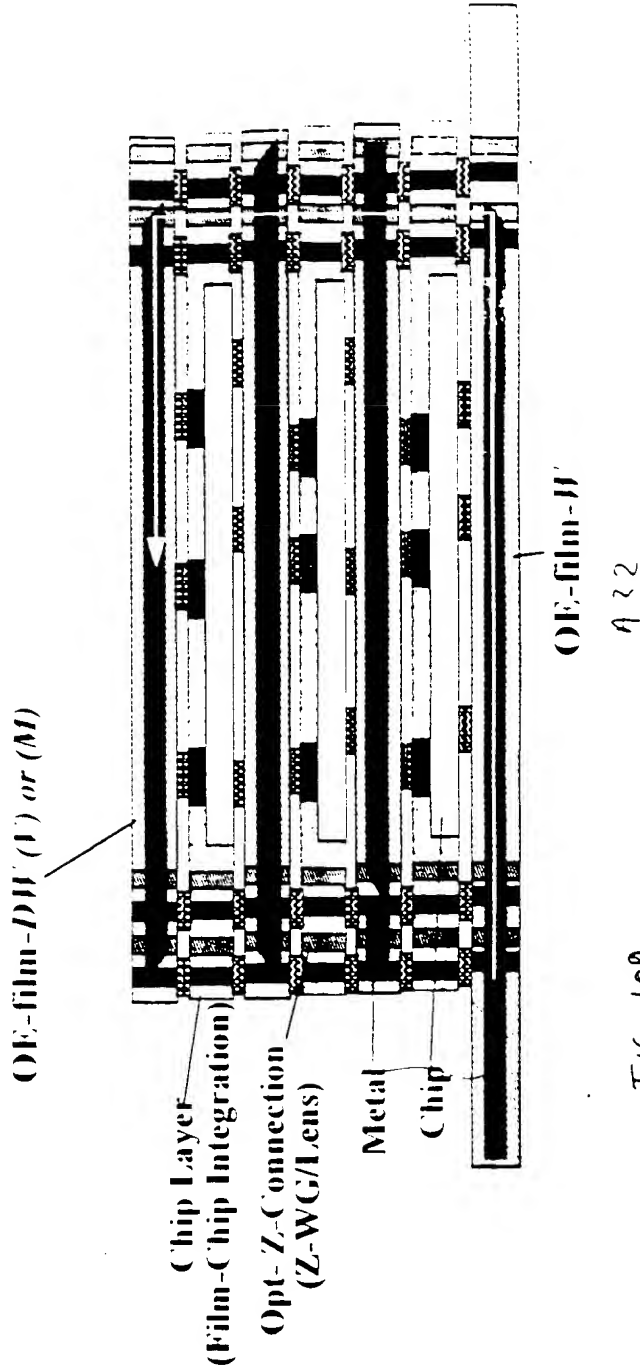
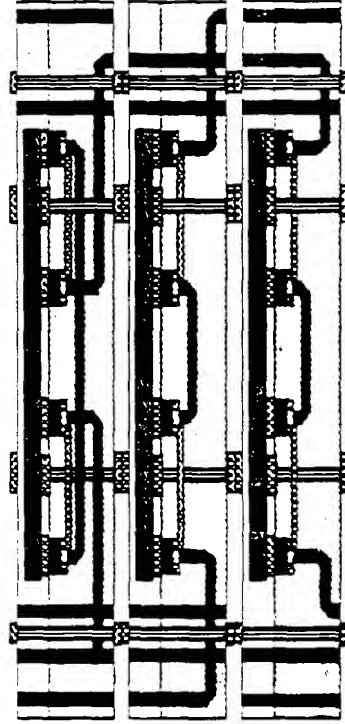
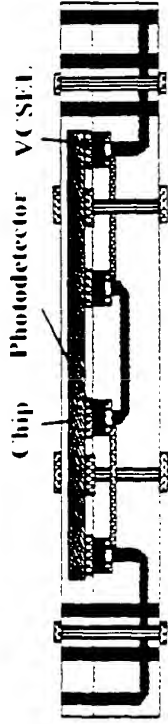


FIG. 109

102270" 28549460



F16.110

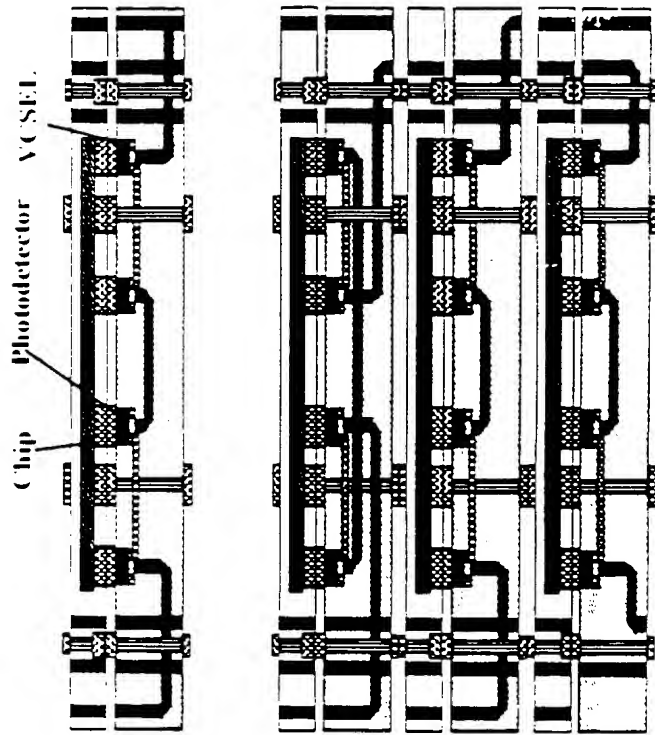
A23

(2/23/99) AA1 Detail picture Example for 3D-stack

(New version of the AA1 of 2/5/99)



102210-28549460



F16.110

A24

(2/23/99) AA2 Detail picture Example for 3D-stack

(New version of the AA2 of 2/5/99)

## Film/Z-Connection Application to OE-Substrate

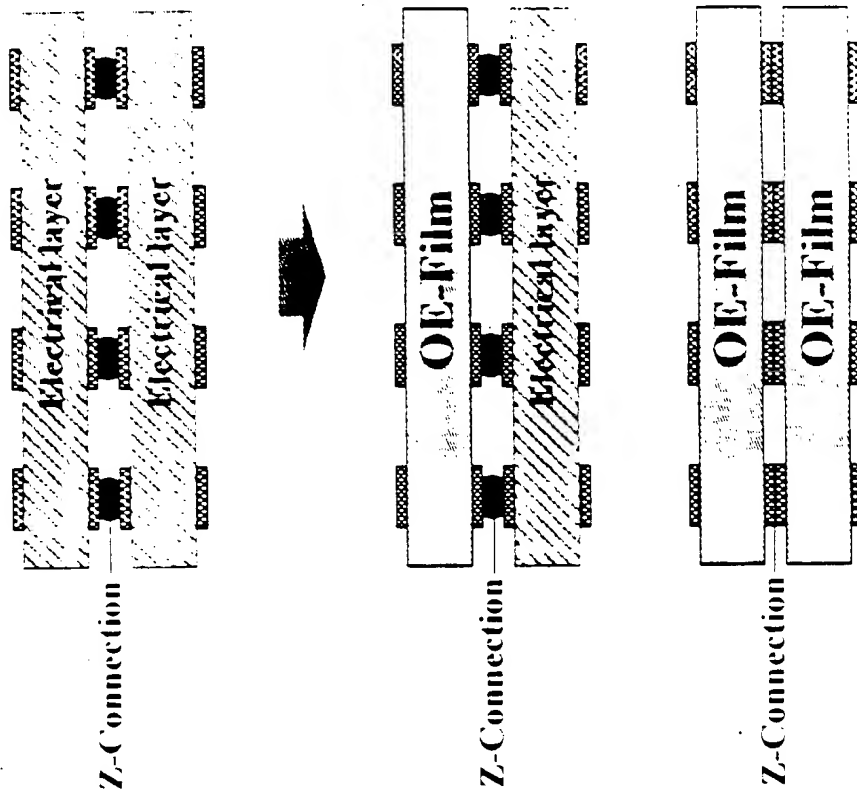
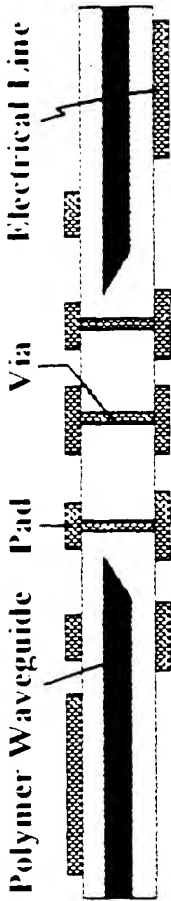


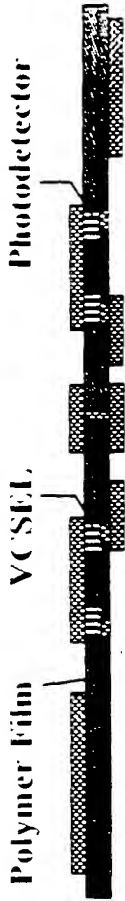
Fig. 11/2

## OE-Films



OE-film-W

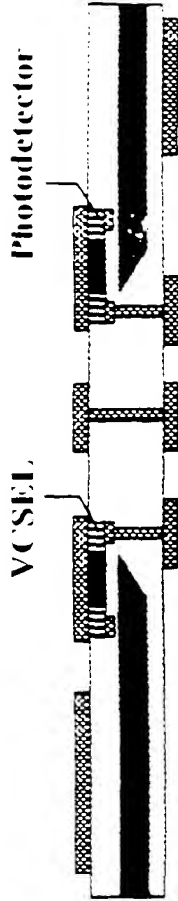
F16.113



OE-film-D

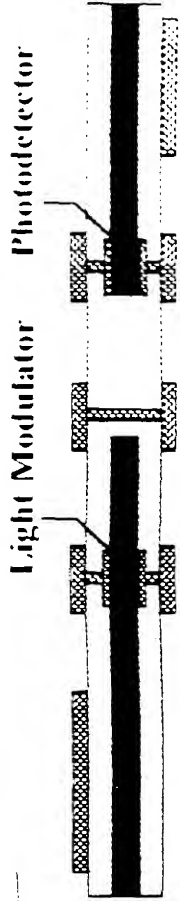
F16.114

A8



OE-film-DW(V)

F16.115



OE-film-DW(M)

2/17/99-added 2

F16.116

100-1711

# FOLM

Fiber Array OE-Film-DIW (1)

Image Guide Waveguide Array

Connector

VCSEL

Chip

Photodetector

Chip

Electrical-MCM

Electrical Board

Fig. 117

A 9

Z-connection

Infr-type

OE-Film-D

OE-Film-W

Chip

Chip

Electrical-MCM

Electrical Board

Z-connection

IP-type

(2/23/99) Fig. No. 14 Modified divided 1/4

Fig. 118

A 9 2/23/99

# FOLM

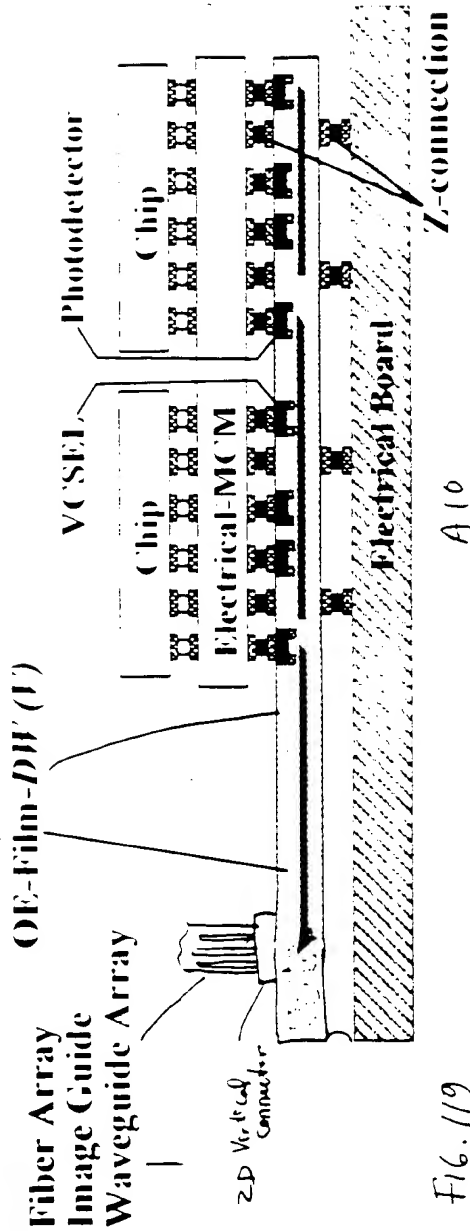
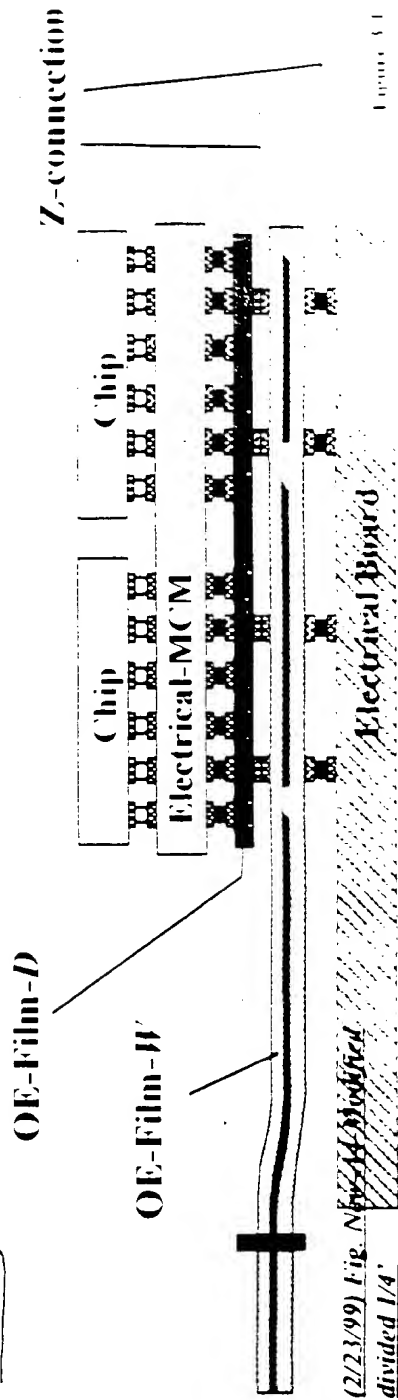


Fig. 119



(2/23/99) Fig. 120 Modified divided 1/4'

**FUJITSU** Computer Packaging Technologies, Inc. **FCPT**  
**FOLM with Optical Path Length Controller, Connector Buffer**

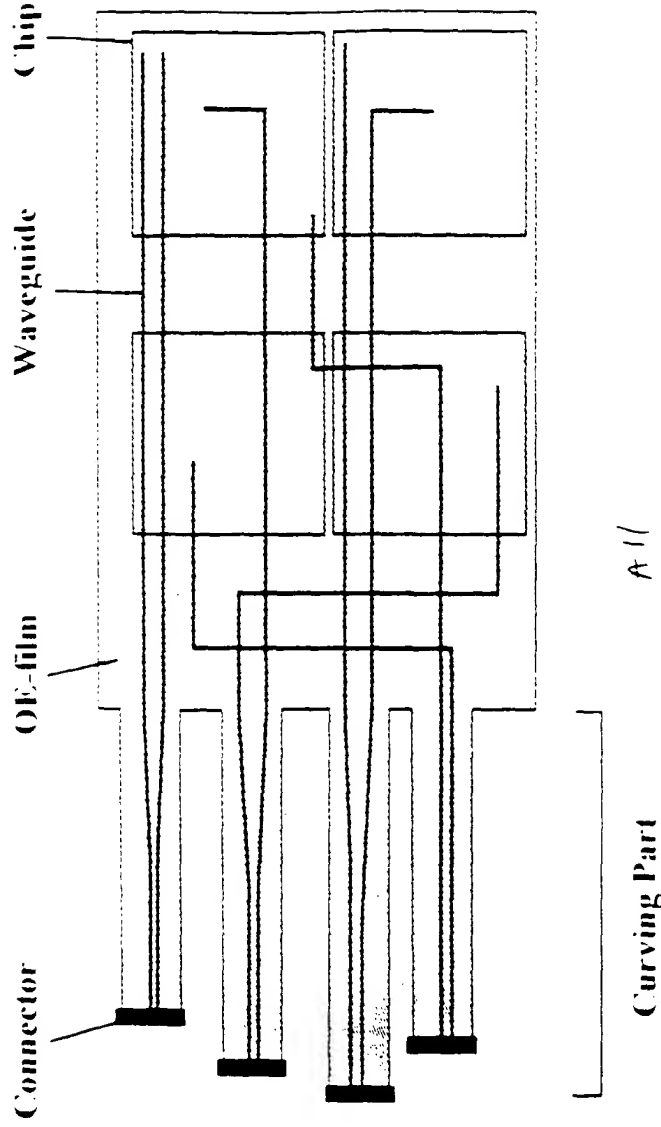


Fig. 121

(2/17/99) Fig. New-A4 Modified  
 divided 2/4

**FUJITSU** Computer Packaging Technologies, Inc. **FCPT**  
**FOLM with Optical Path Length Controller, Connector Buffer**

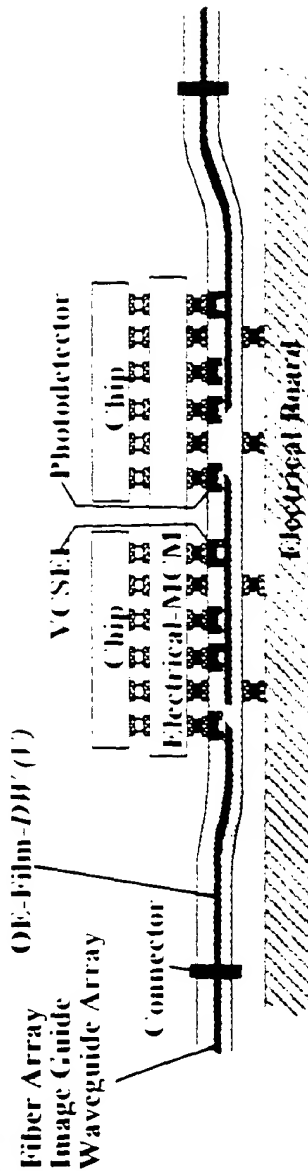


Fig. 123

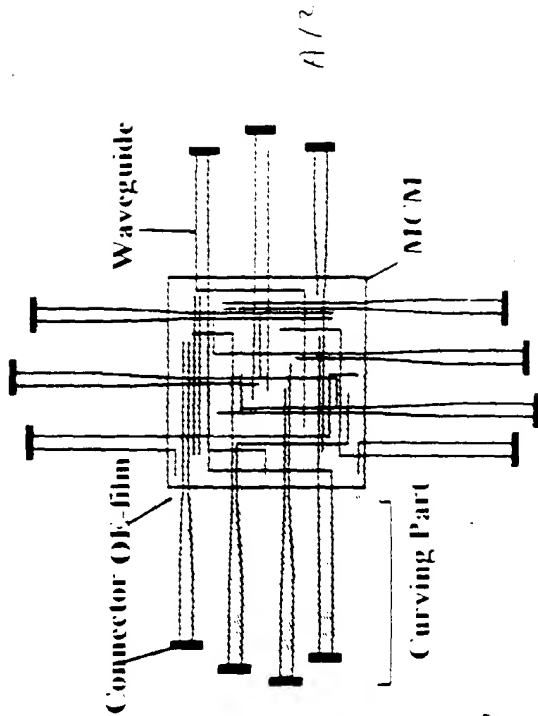
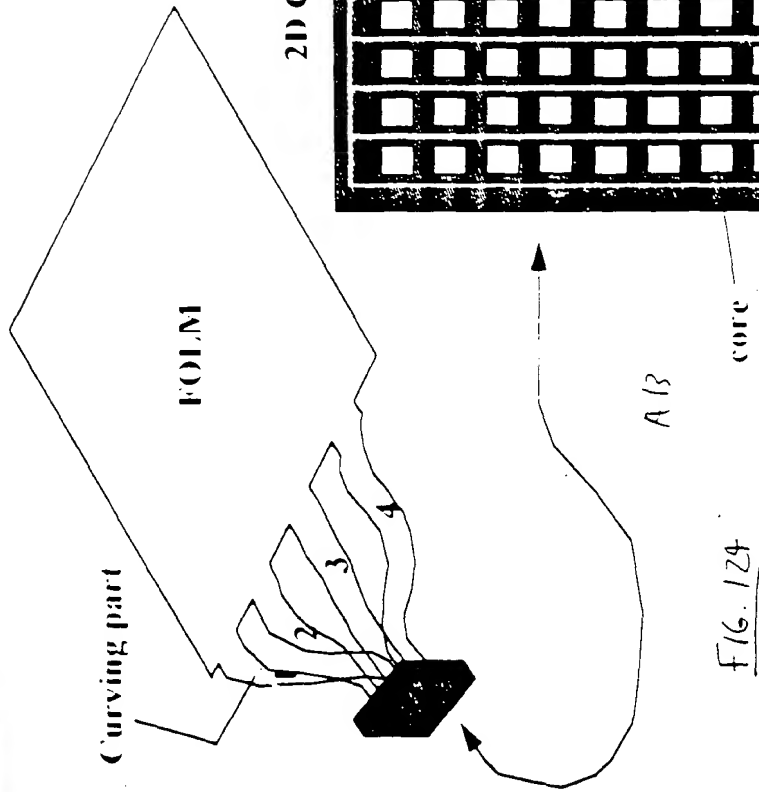


Fig. 122

(2/23/99) Fig. New-A4-Modified  
 divided 2/4'

**FOLM with 2D Waveguide Connector**FIG. 124(2/23/99) Fig. New-44-Modified  
divided 1/4'

(for Single-layer waveguide) (for 2 layer waveguide) (continued)



## FOLM: High-Speed Option

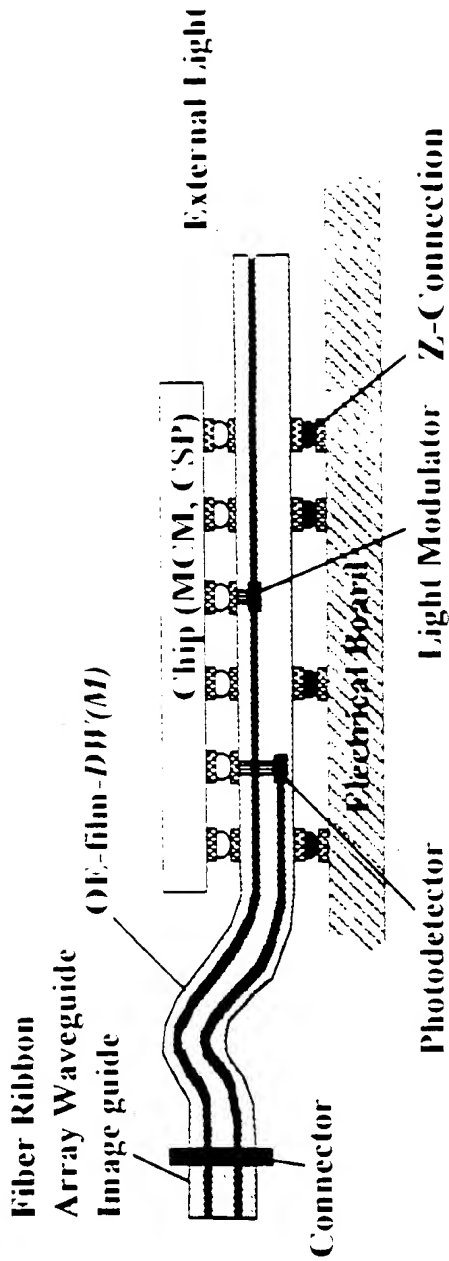


Fig. 125

A 14



# FOLM Structure Example (VCSEL part)

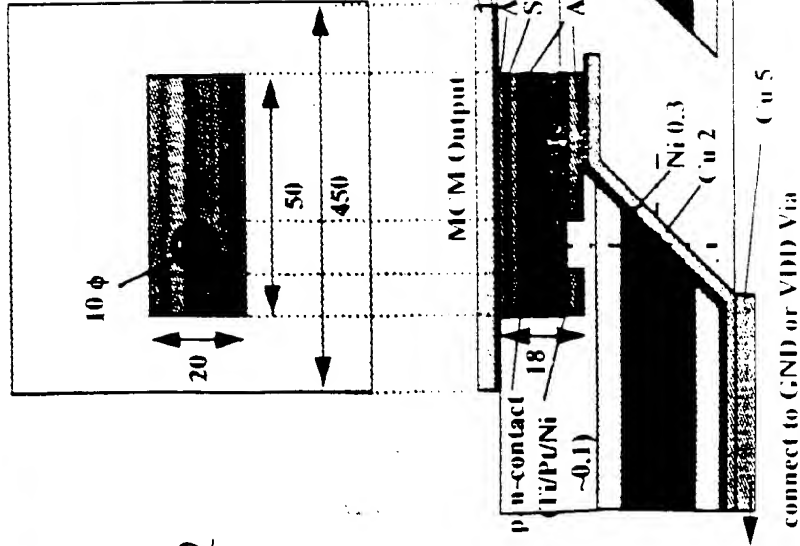


fig. 129

fig. 128

Unit : um

# OE-film: OE-IP, OE-Film-MCM

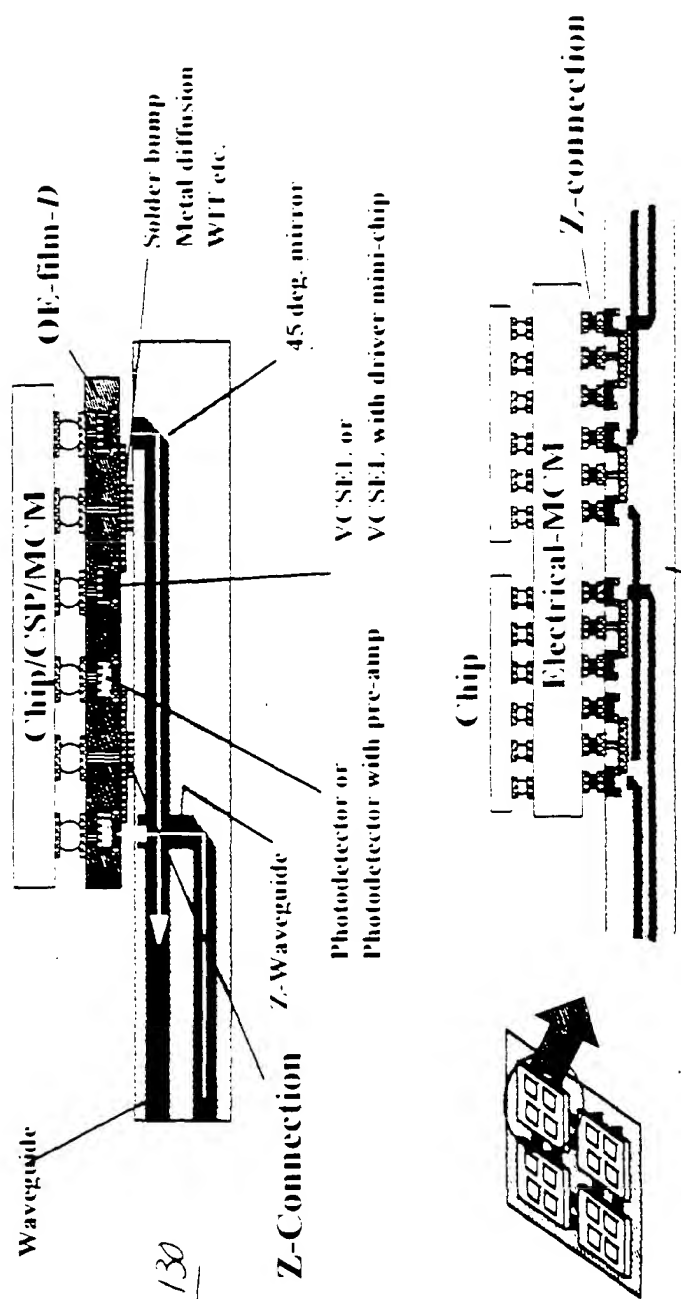


Fig. 130

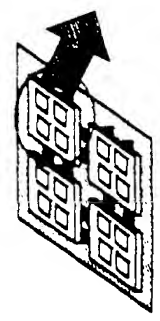
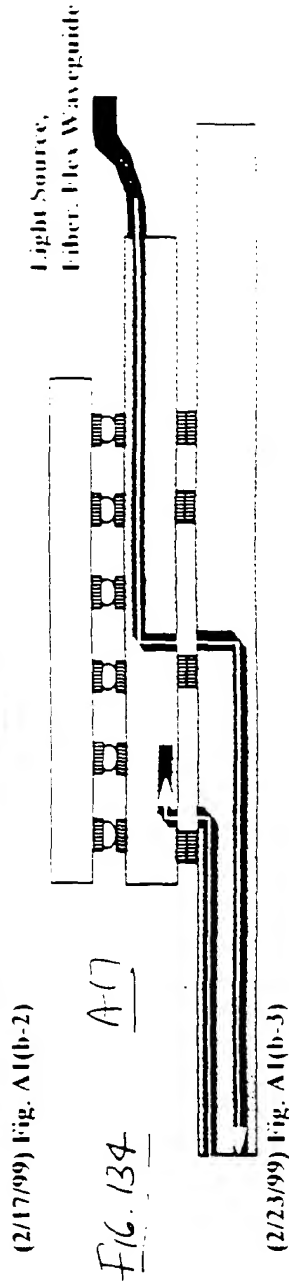
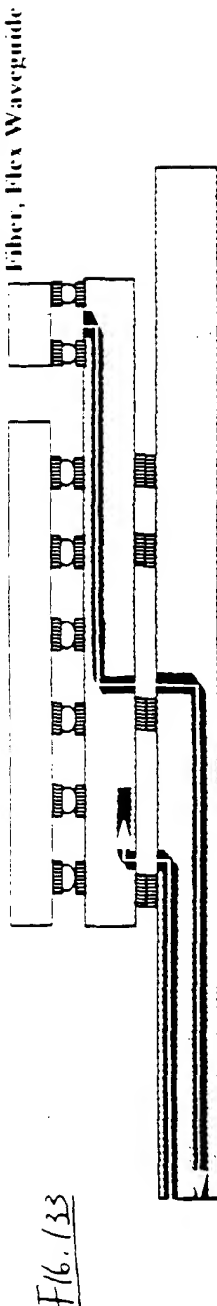
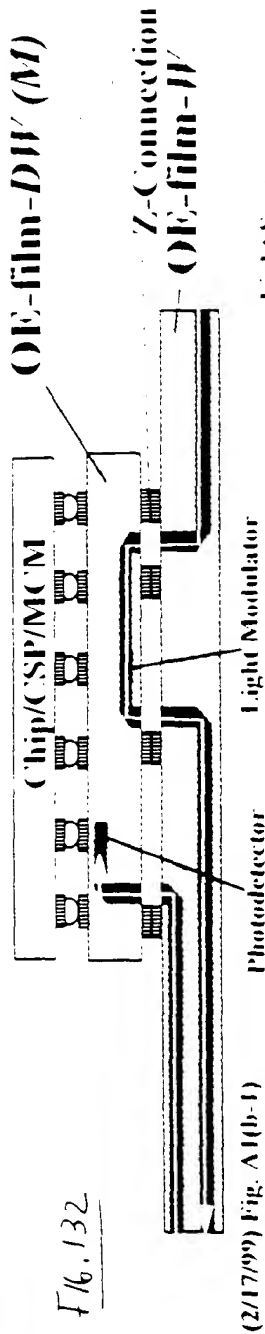


Fig. 131 A 15 OE-film-DW (V)

(2/23/99) Fig. New-A1-Modified

# OE-film: Light Modulator Transmitters



# OE-film: Both-Side Packaging

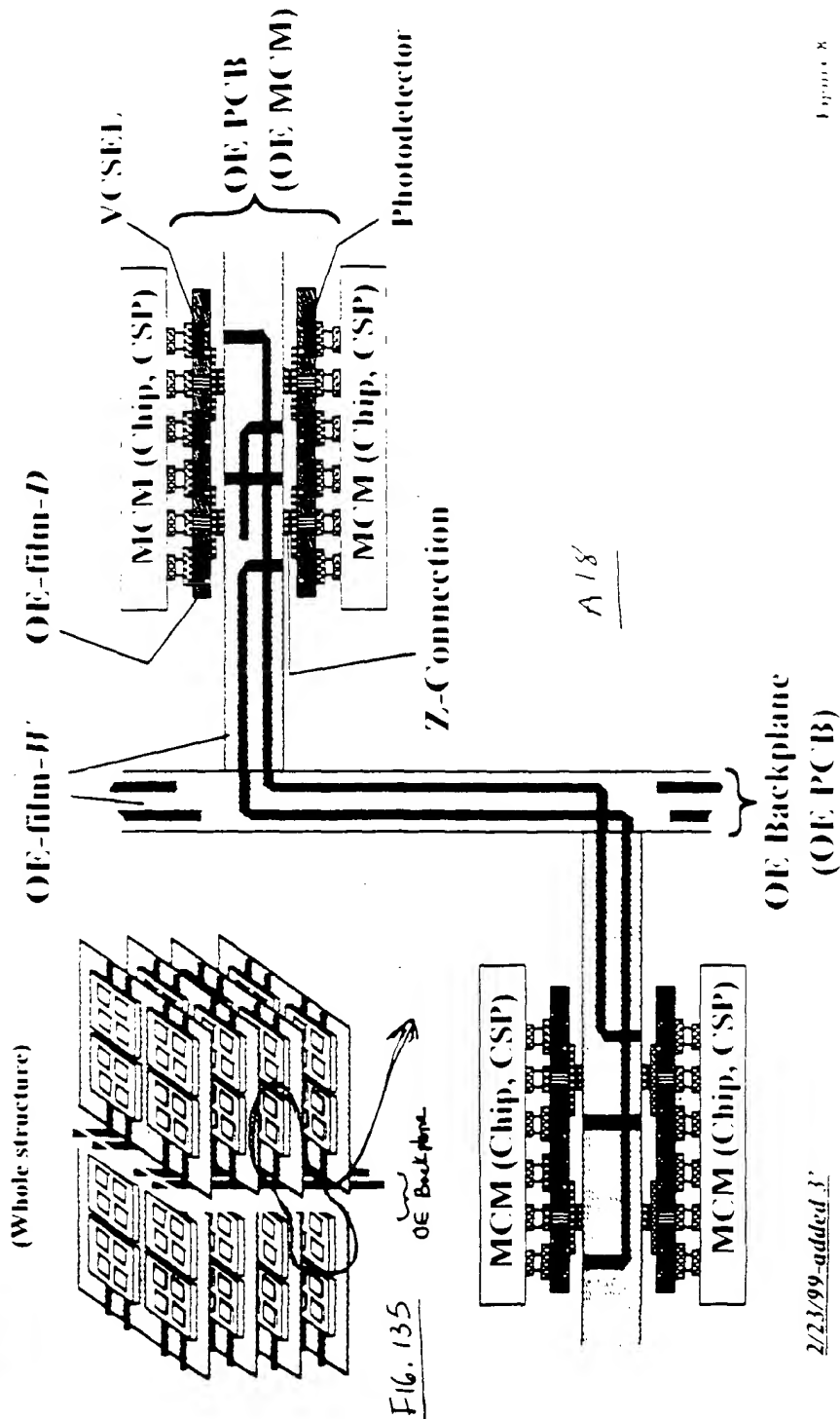
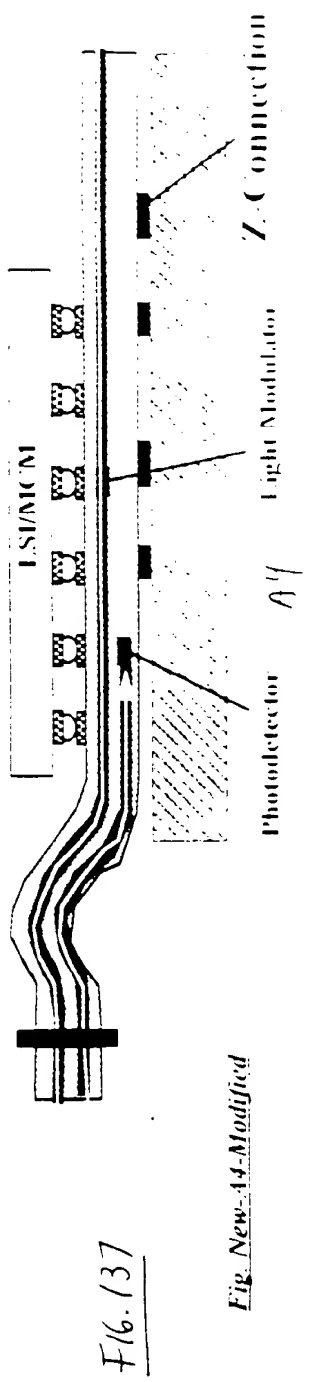
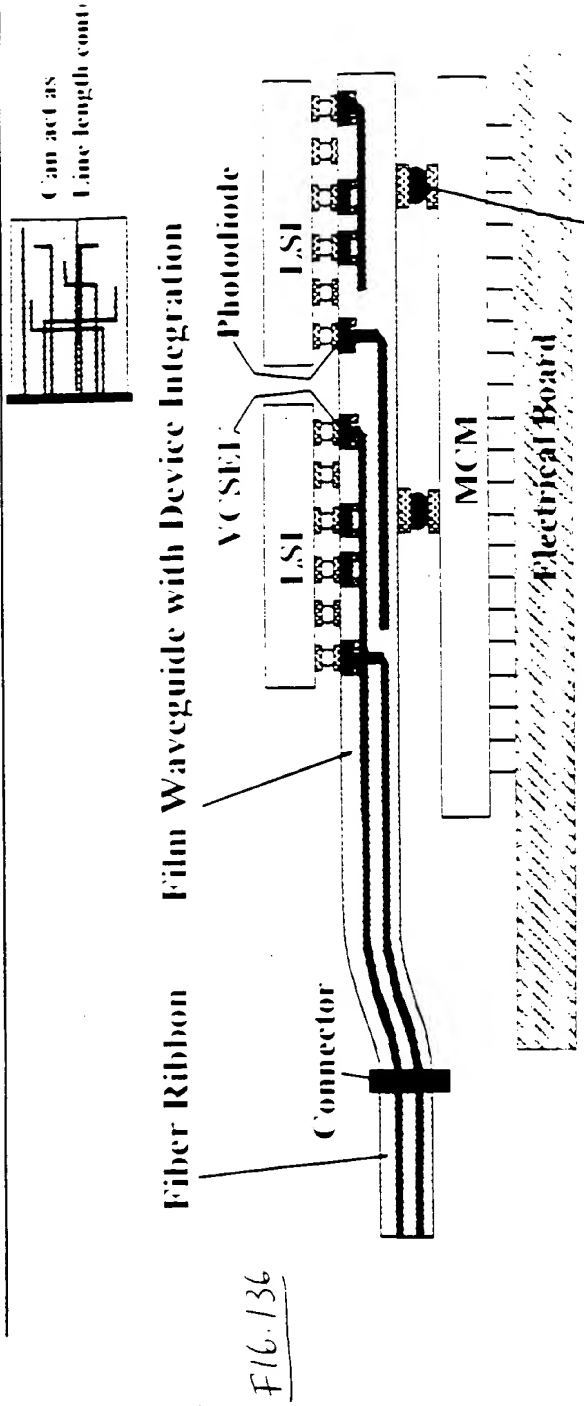
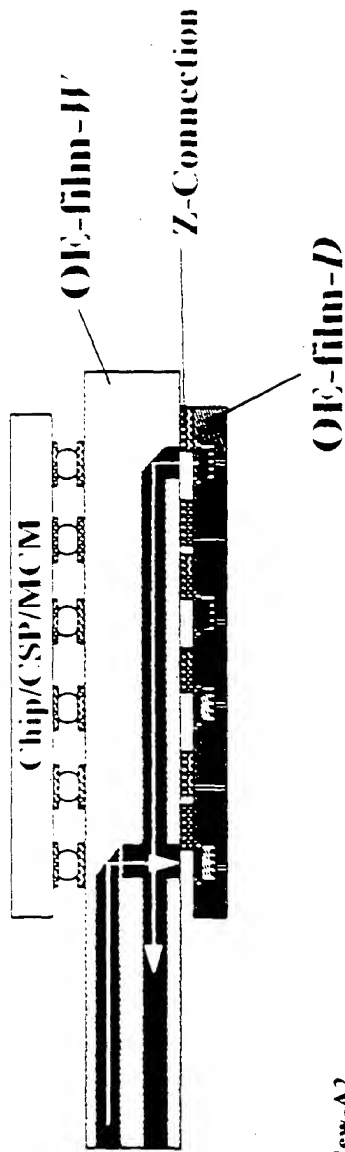


FIG. 135



# OE IP is Placed on the Opposit Side



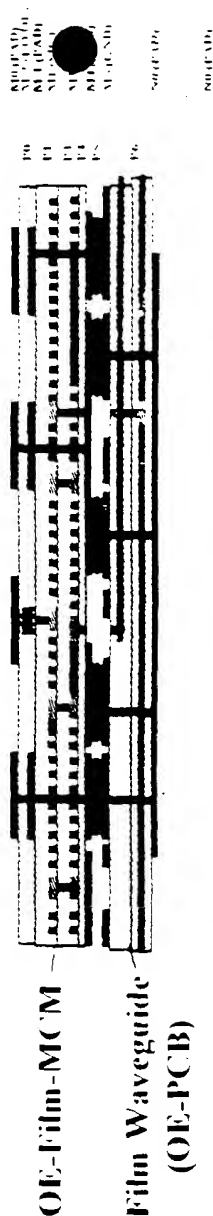
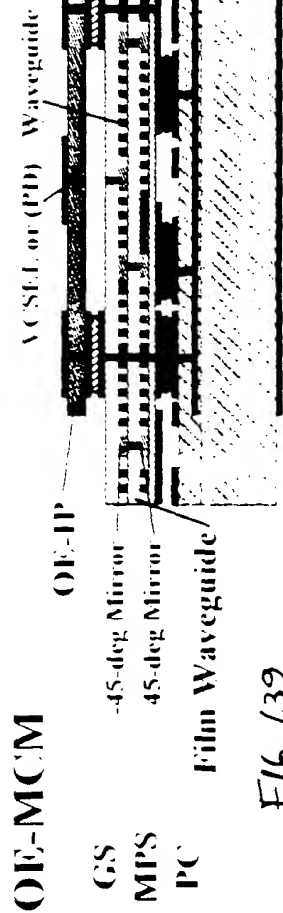
(2/23/99) Fig. New-A2

FL6.138

A2°



# OLE MCM



**Fig. A5-Modific**

FUJITSU Computer Packaging Technologies, Inc. — FCPT  
**OE-film: Smart Pixel**

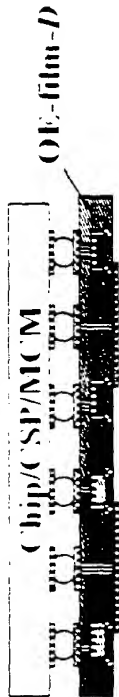
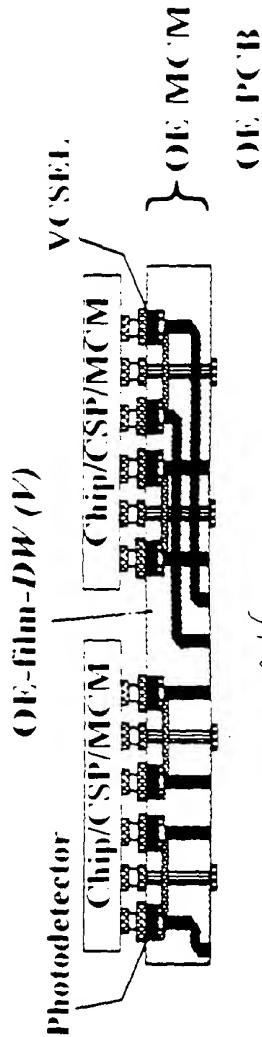


Fig. 141



A16

Fig. 142

# OE-Film/OE-Film Stack --- Back-Side Connection

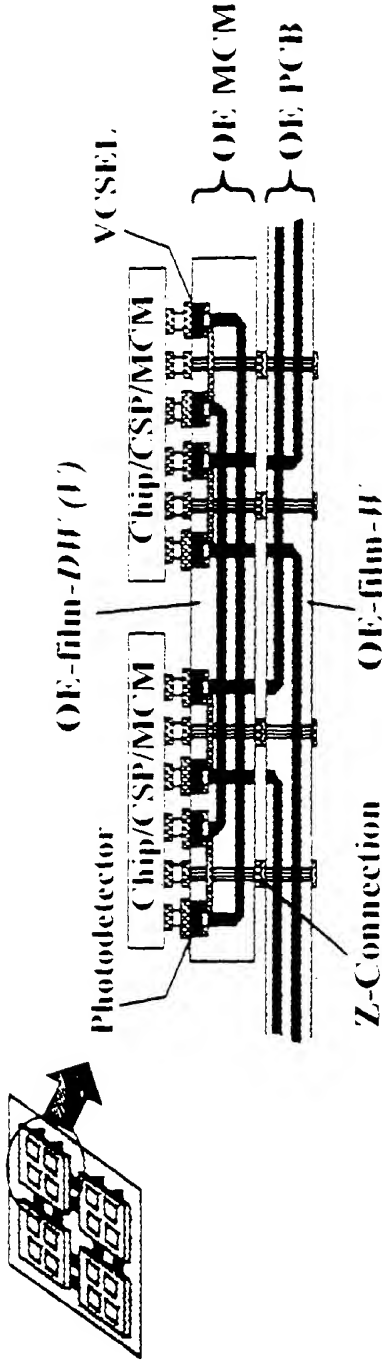
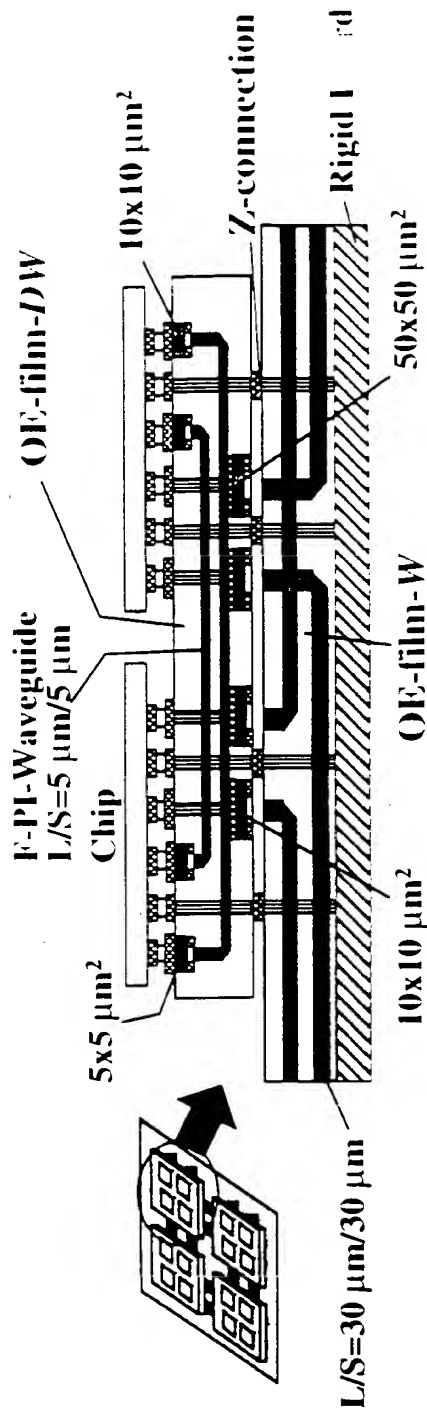


FIG. 143

A19

## OE-Film/OE-Film Stack --- Back-Side Connection



F16.144

# OE-MCM/OE-Bord Stack

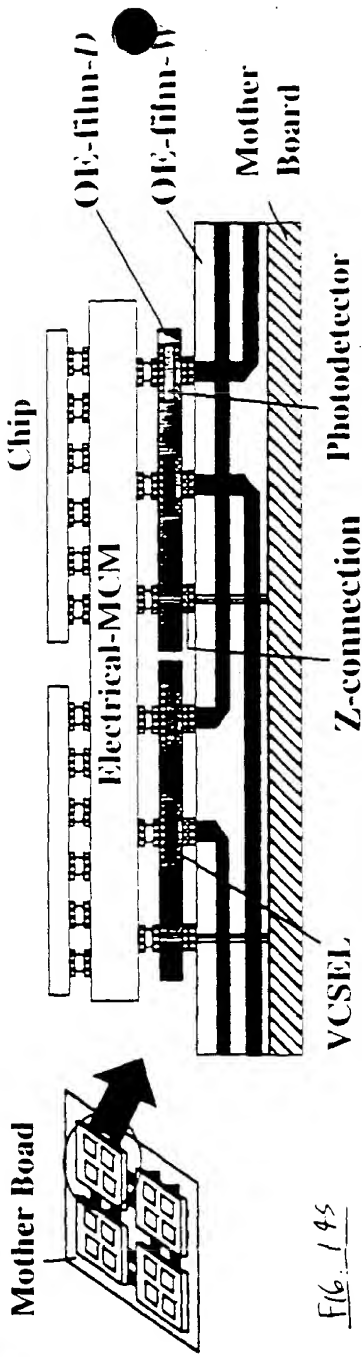


Fig. 145

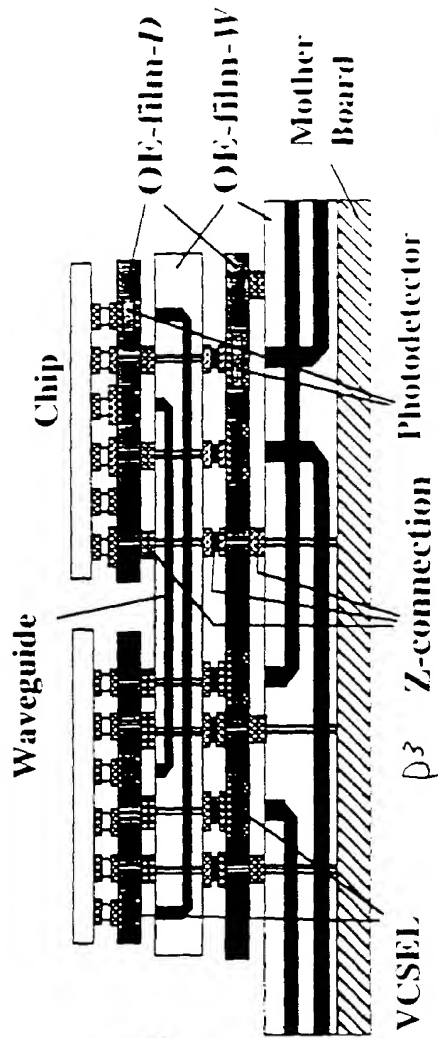
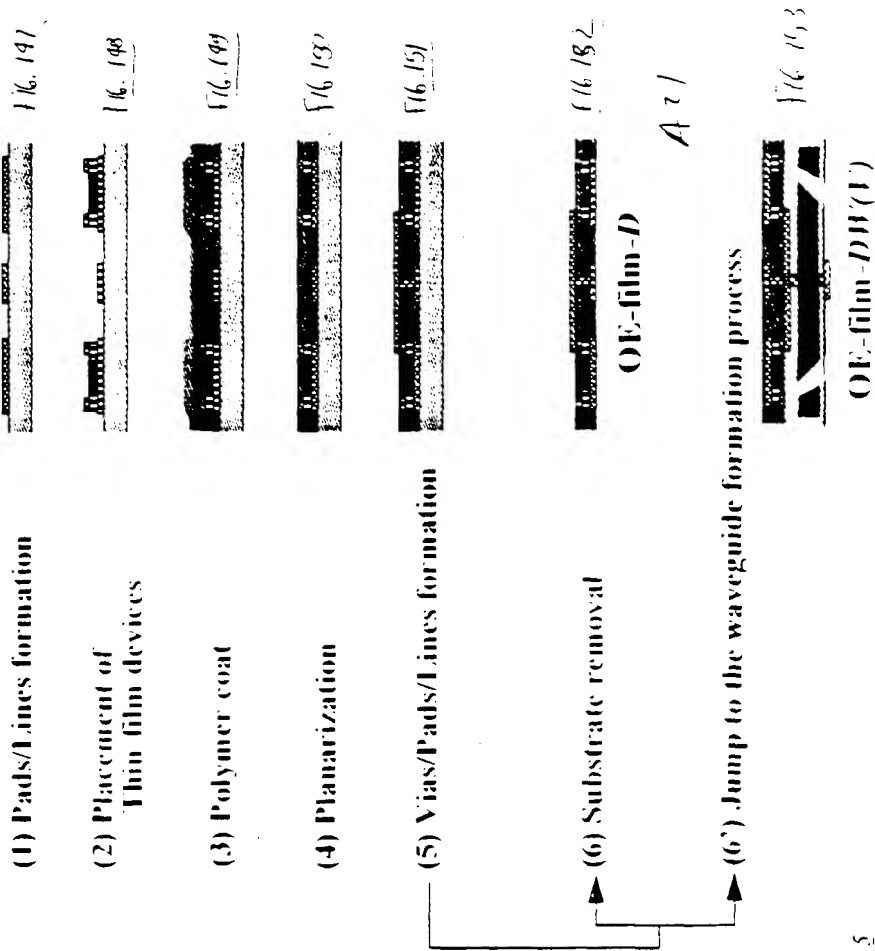


Fig. 3/19/99-1

Fig. 146

## Device Integration Process



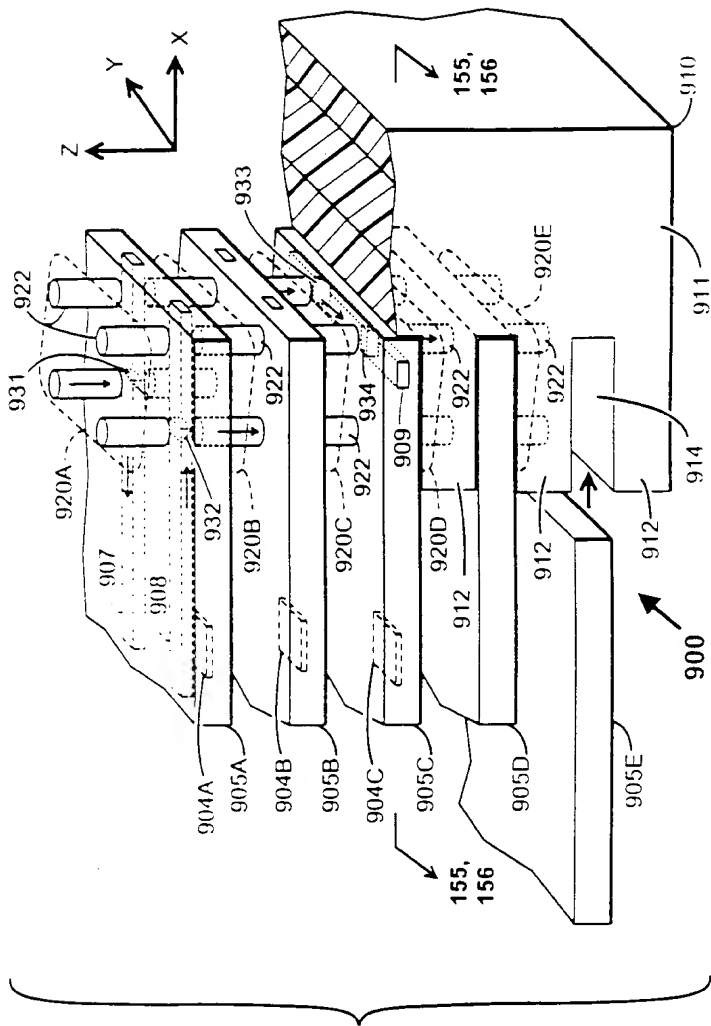


FIG. 154

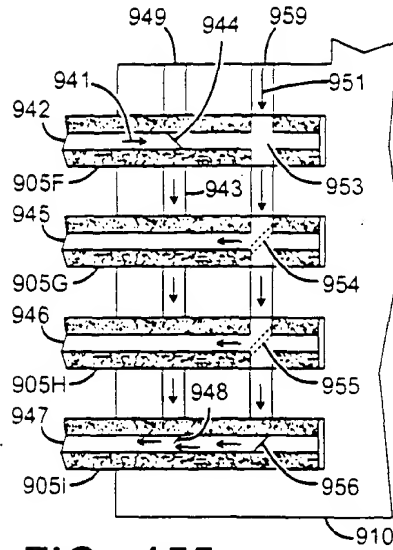


FIG. 155

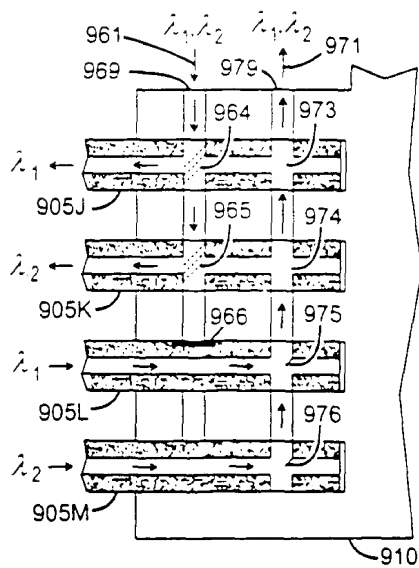


FIG. 156-1

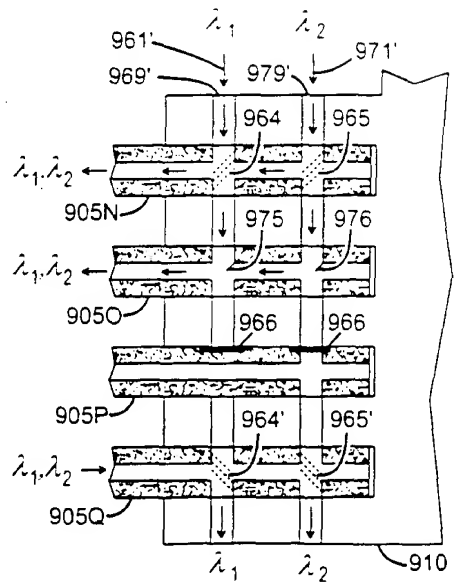
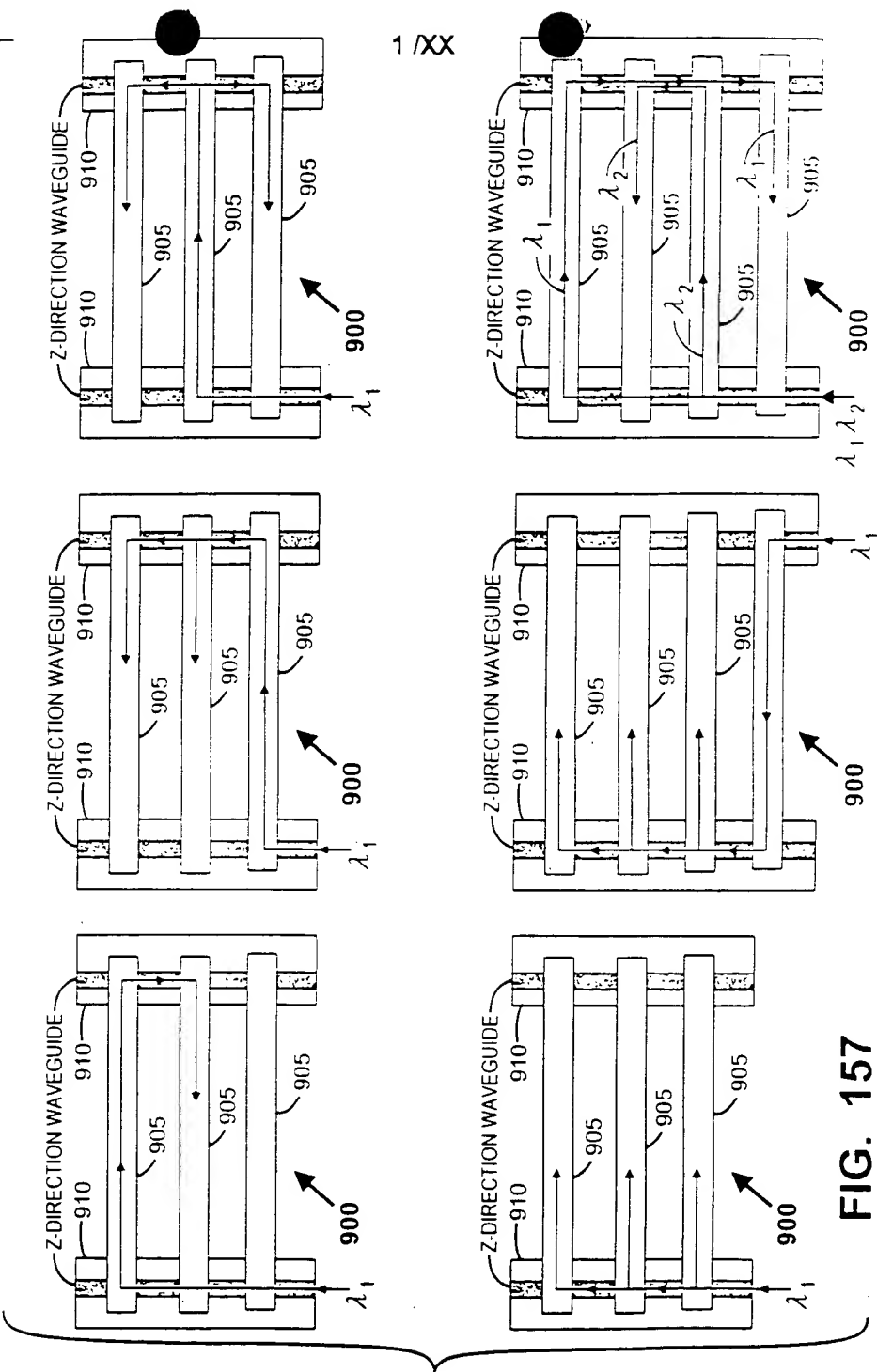


FIG. 156-2





1/XX

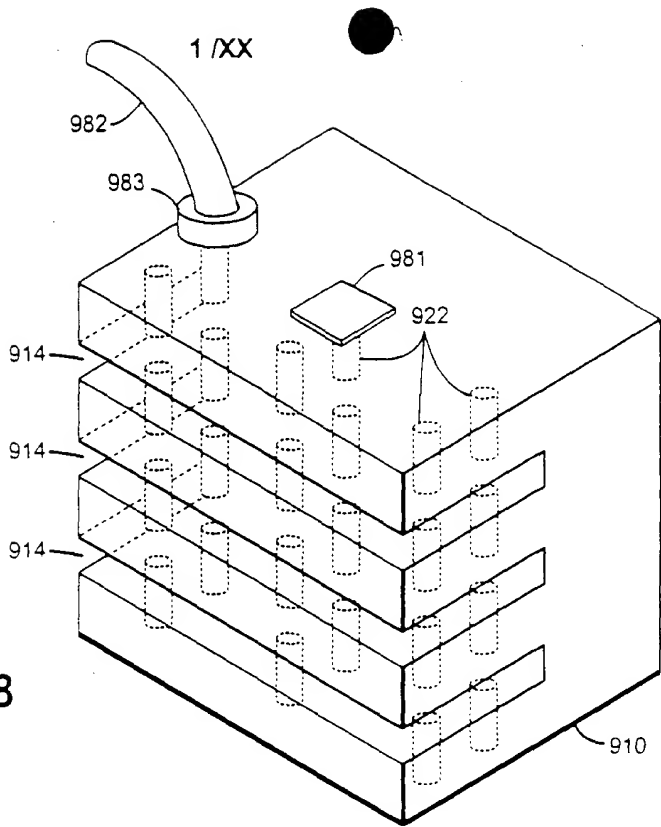


FIG.\_158

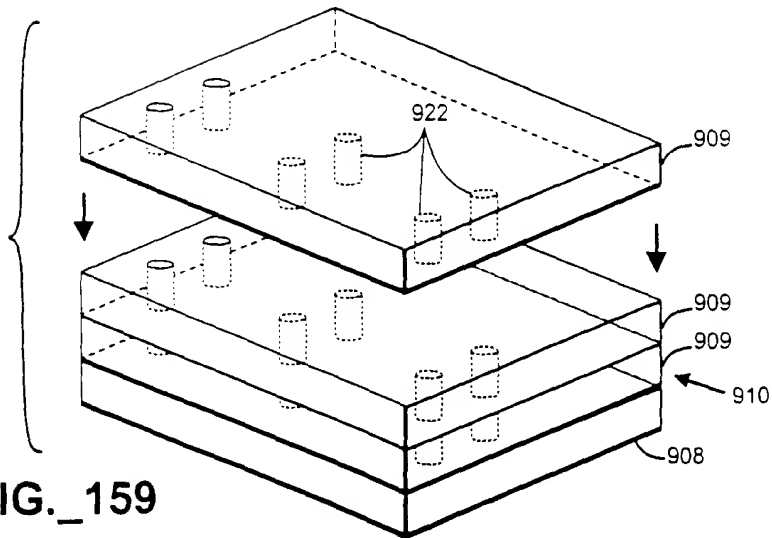


FIG.\_159

09767588.01201

FIG.\_160

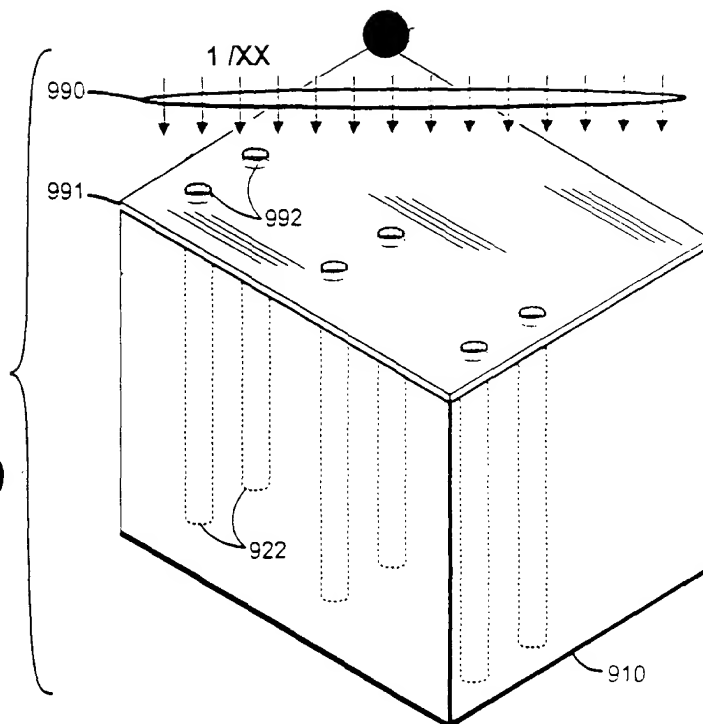
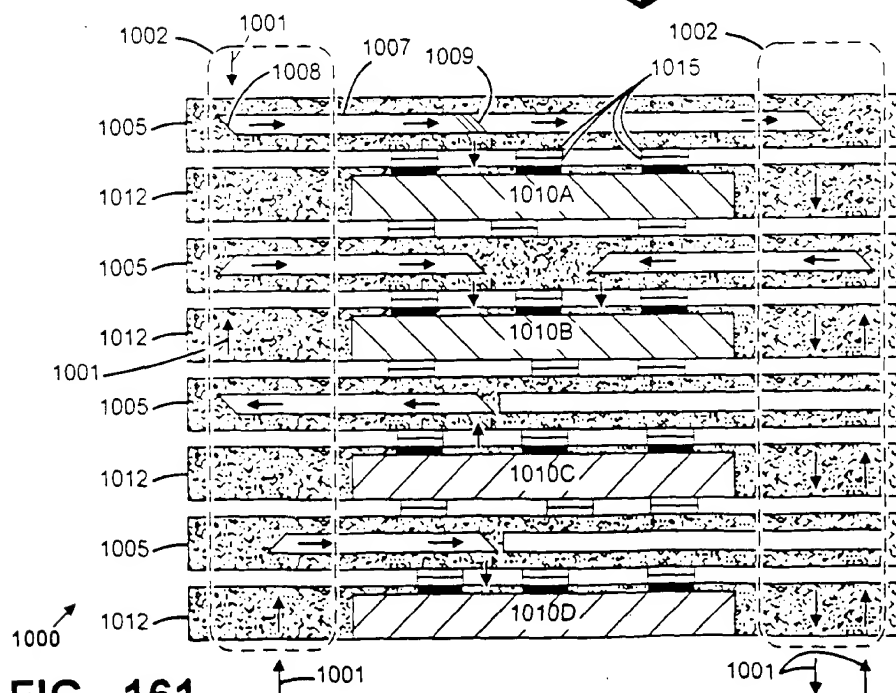
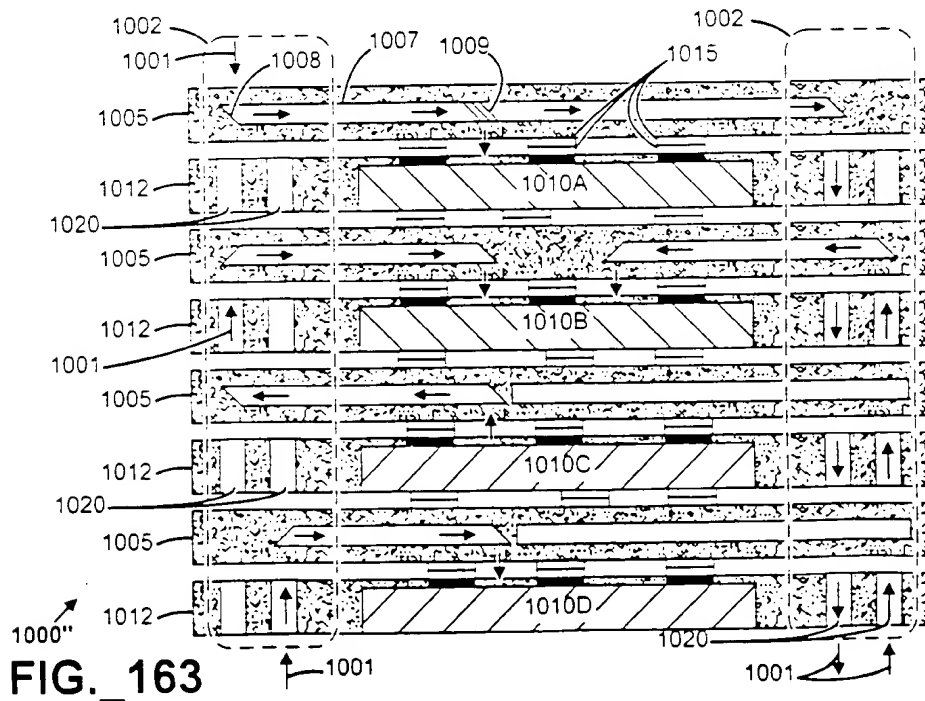
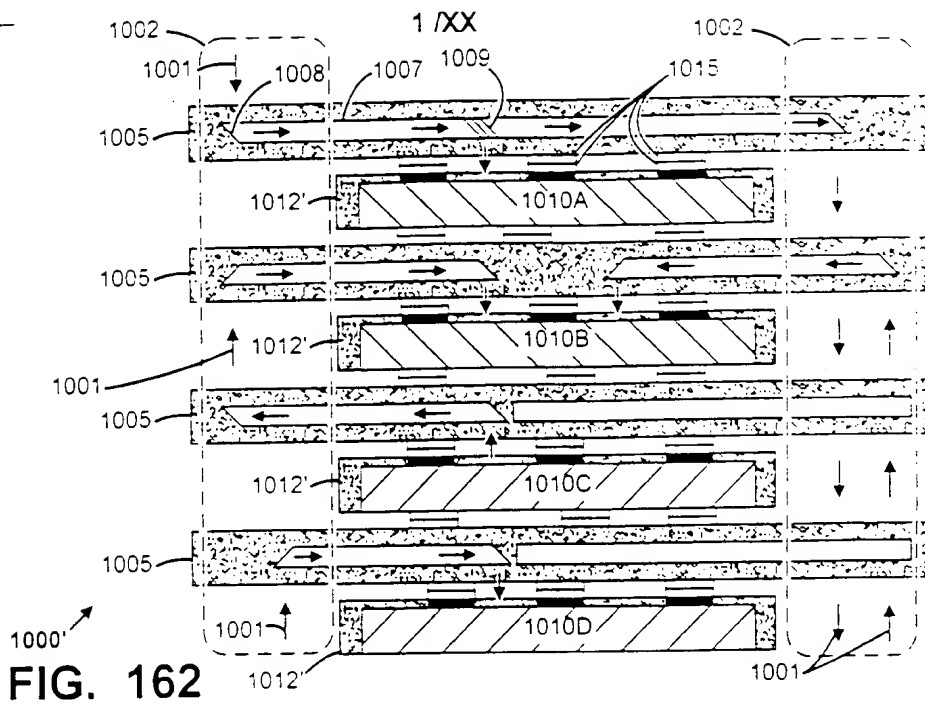
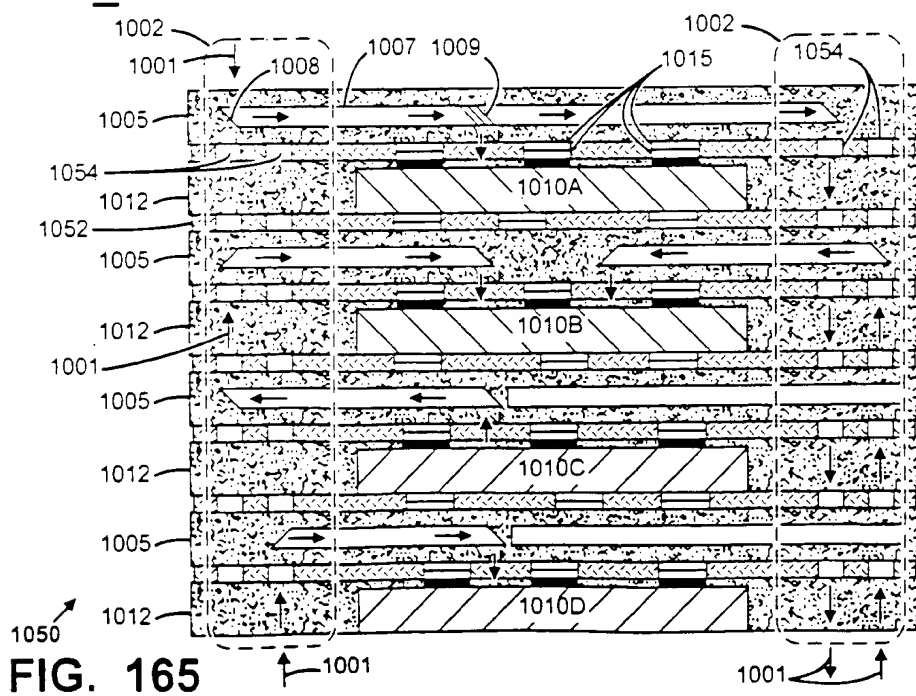
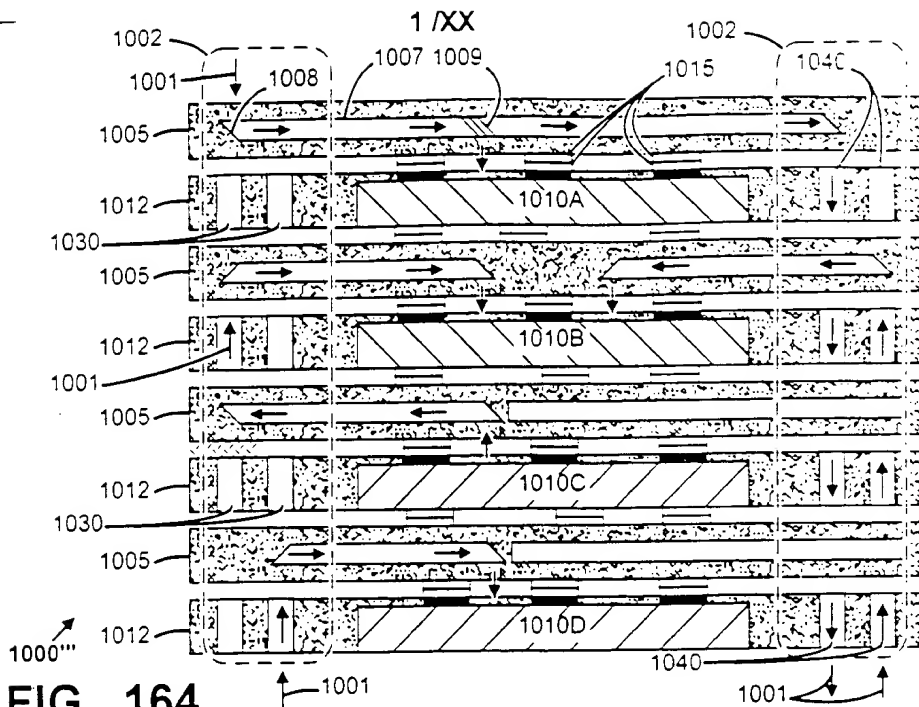


FIG.\_161







00767581 012201

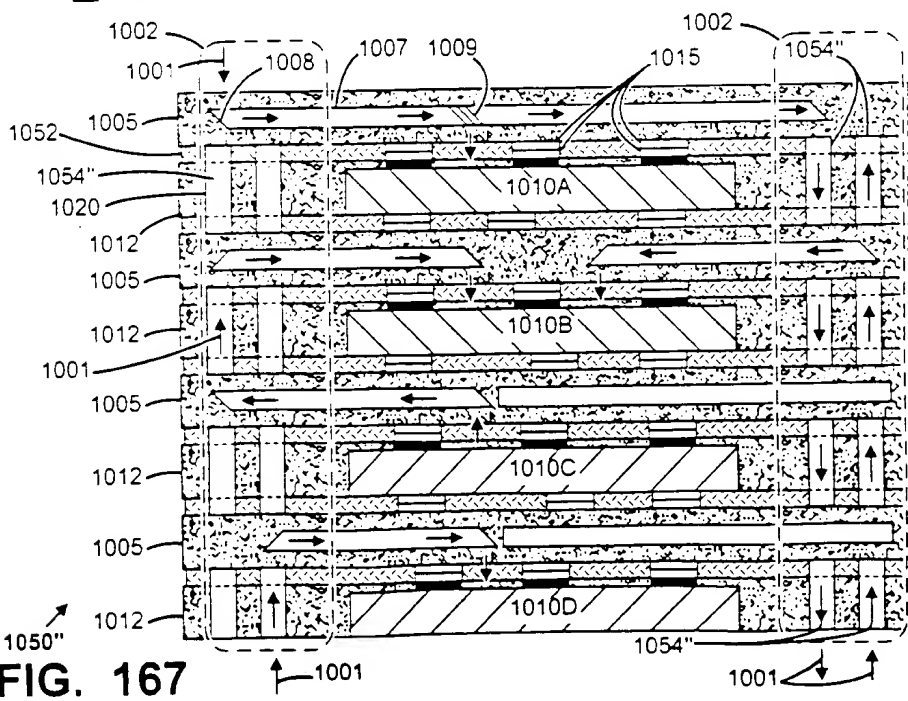
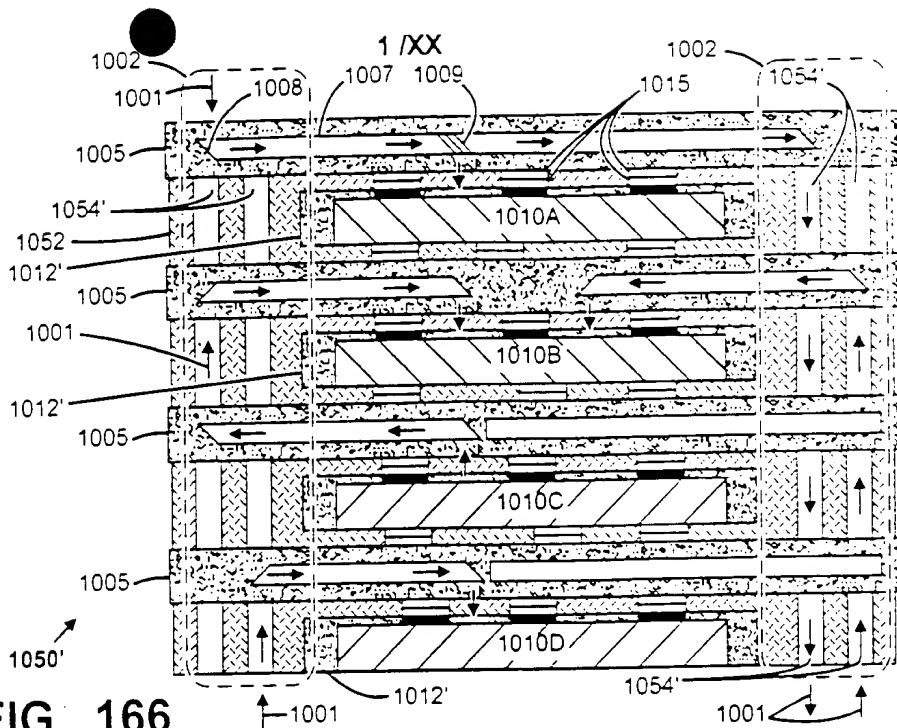
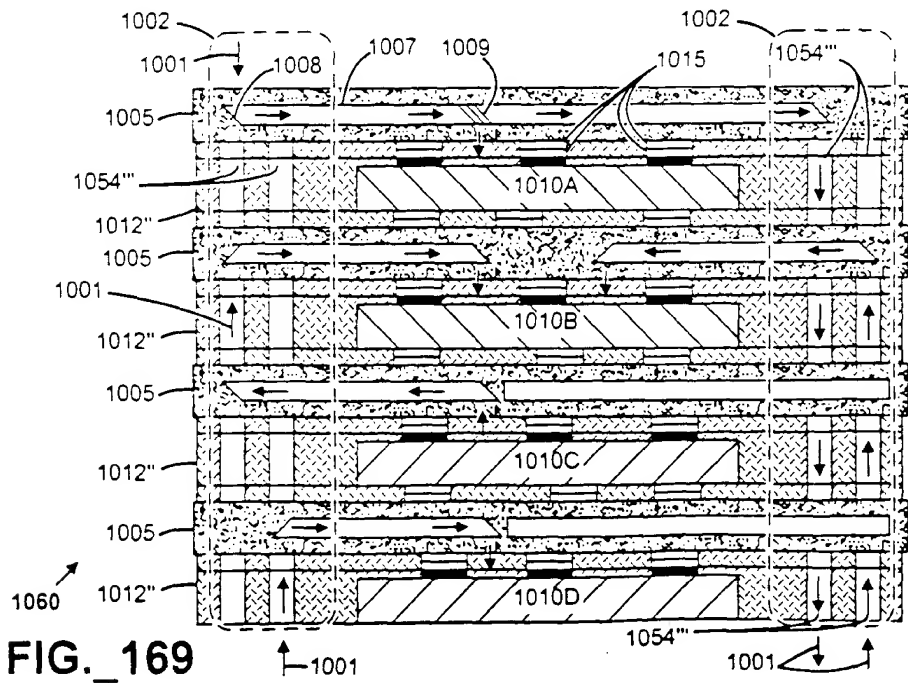
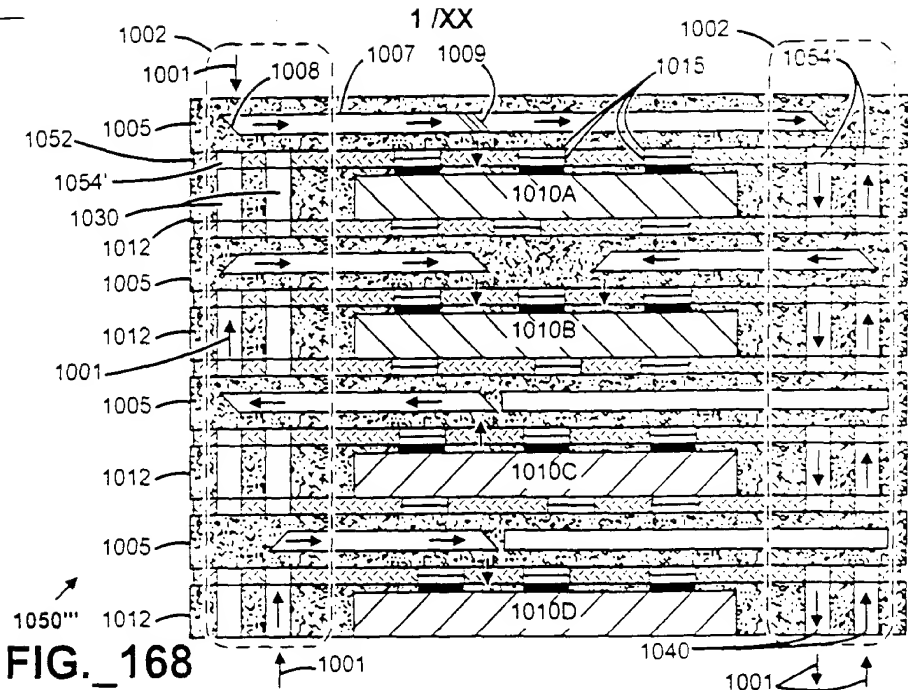


FIG. 166



1/XX

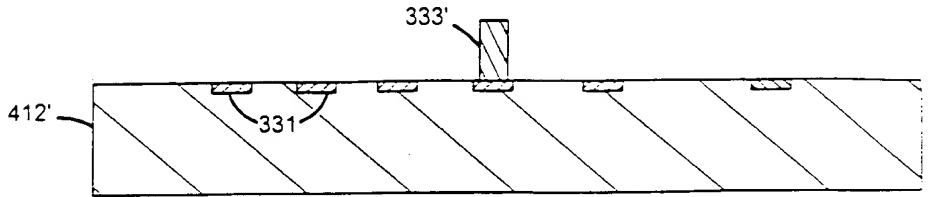


FIG.\_170

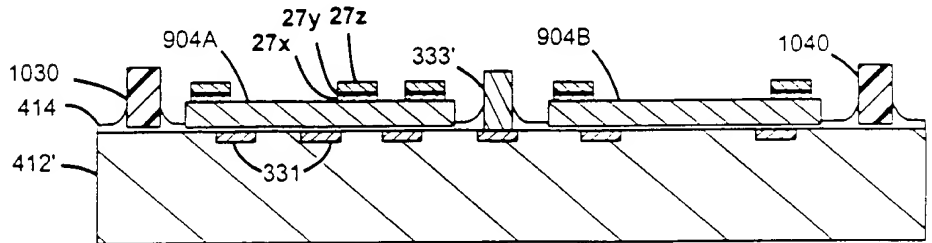


FIG.\_171

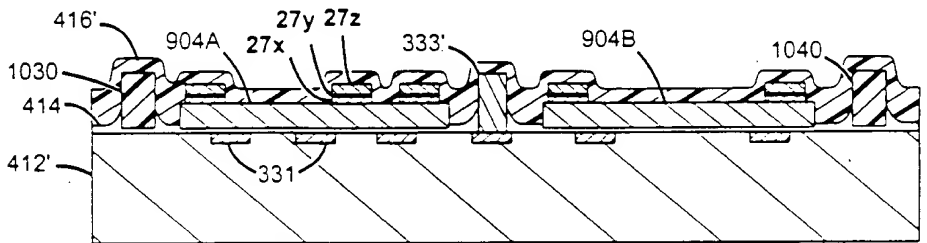


FIG.\_172

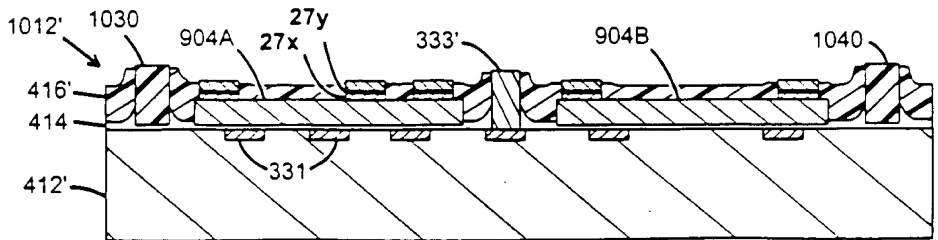


FIG.\_173



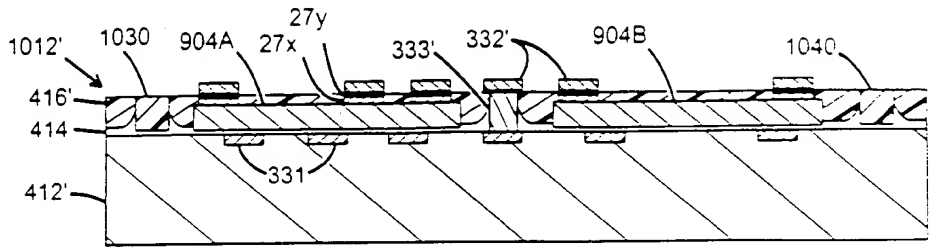


FIG.\_174

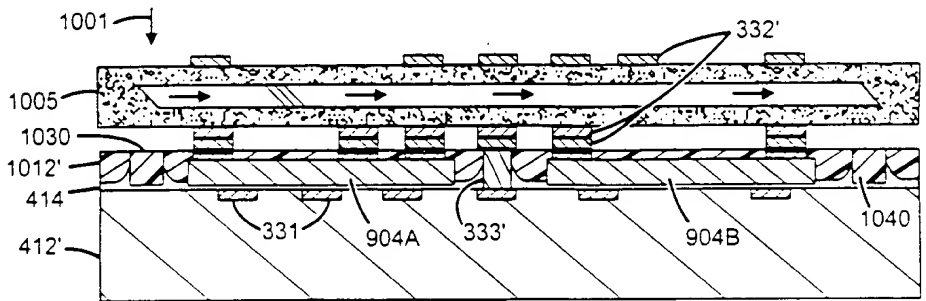


FIG.\_175

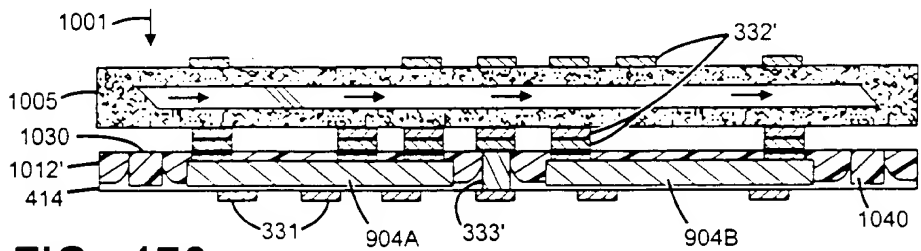


FIG.\_176

1/XX

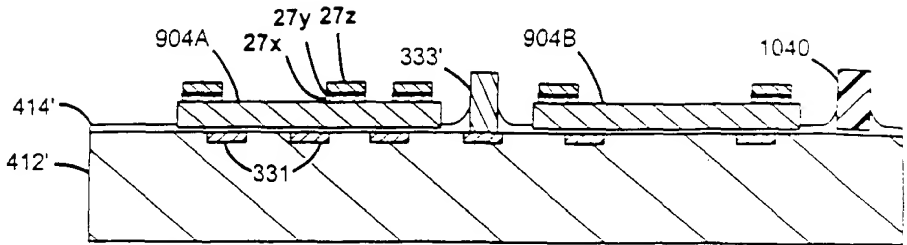


FIG. 177

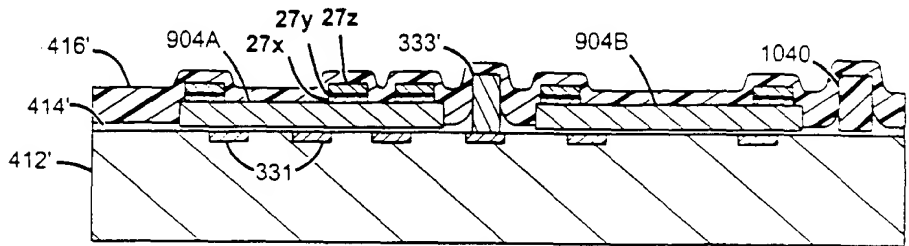


FIG. 178

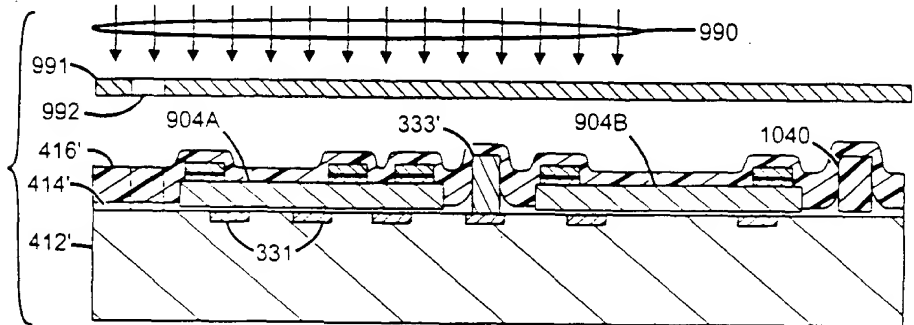


FIG. 179

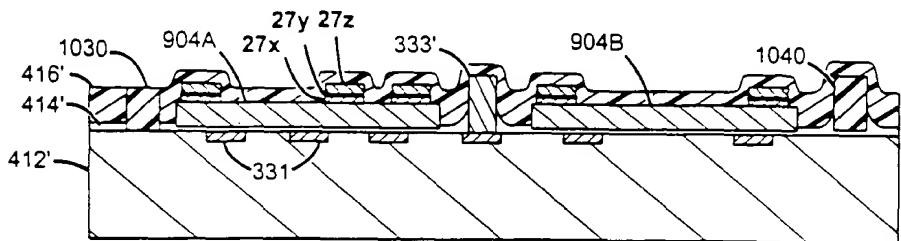
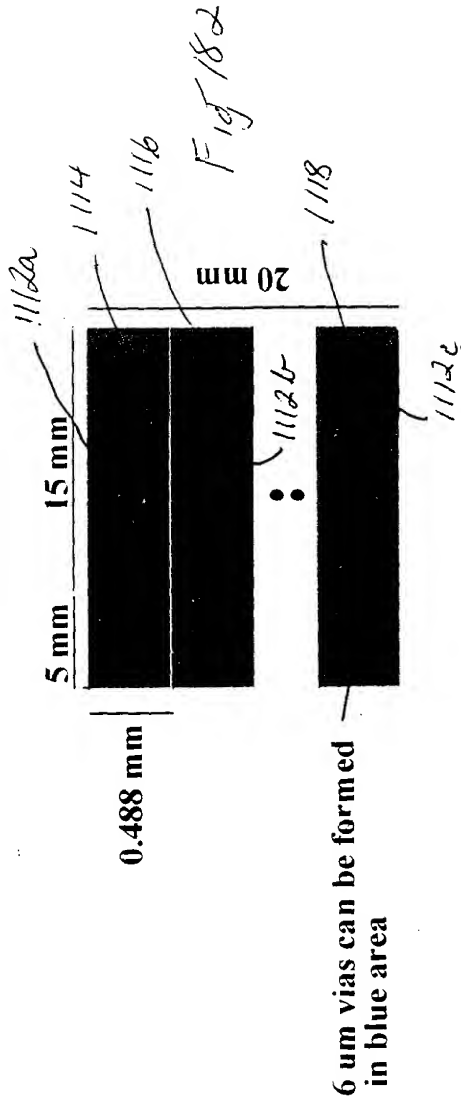
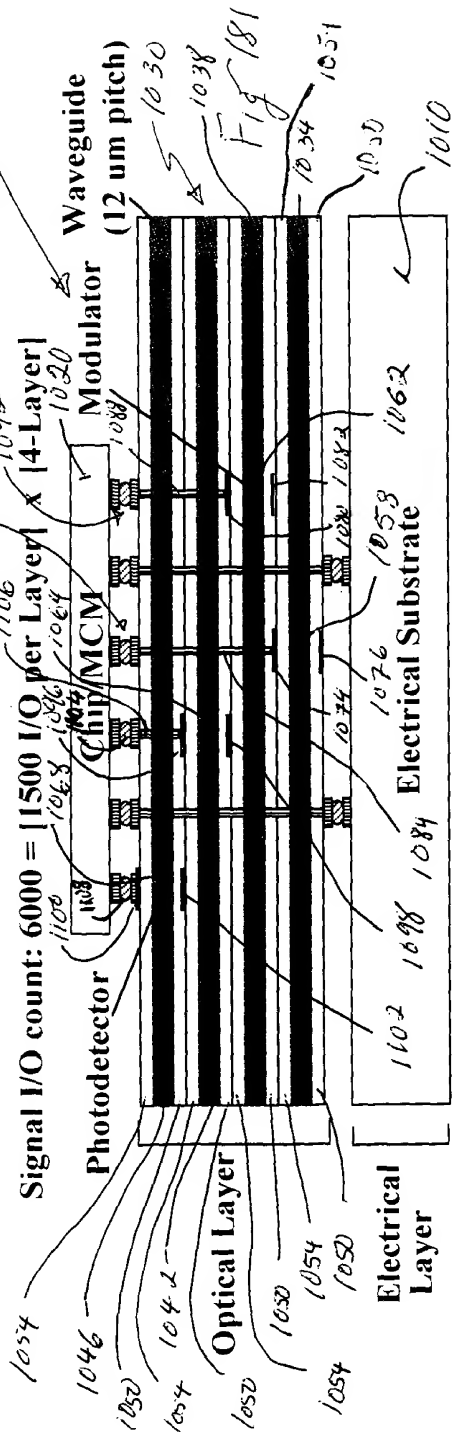


FIG. 180

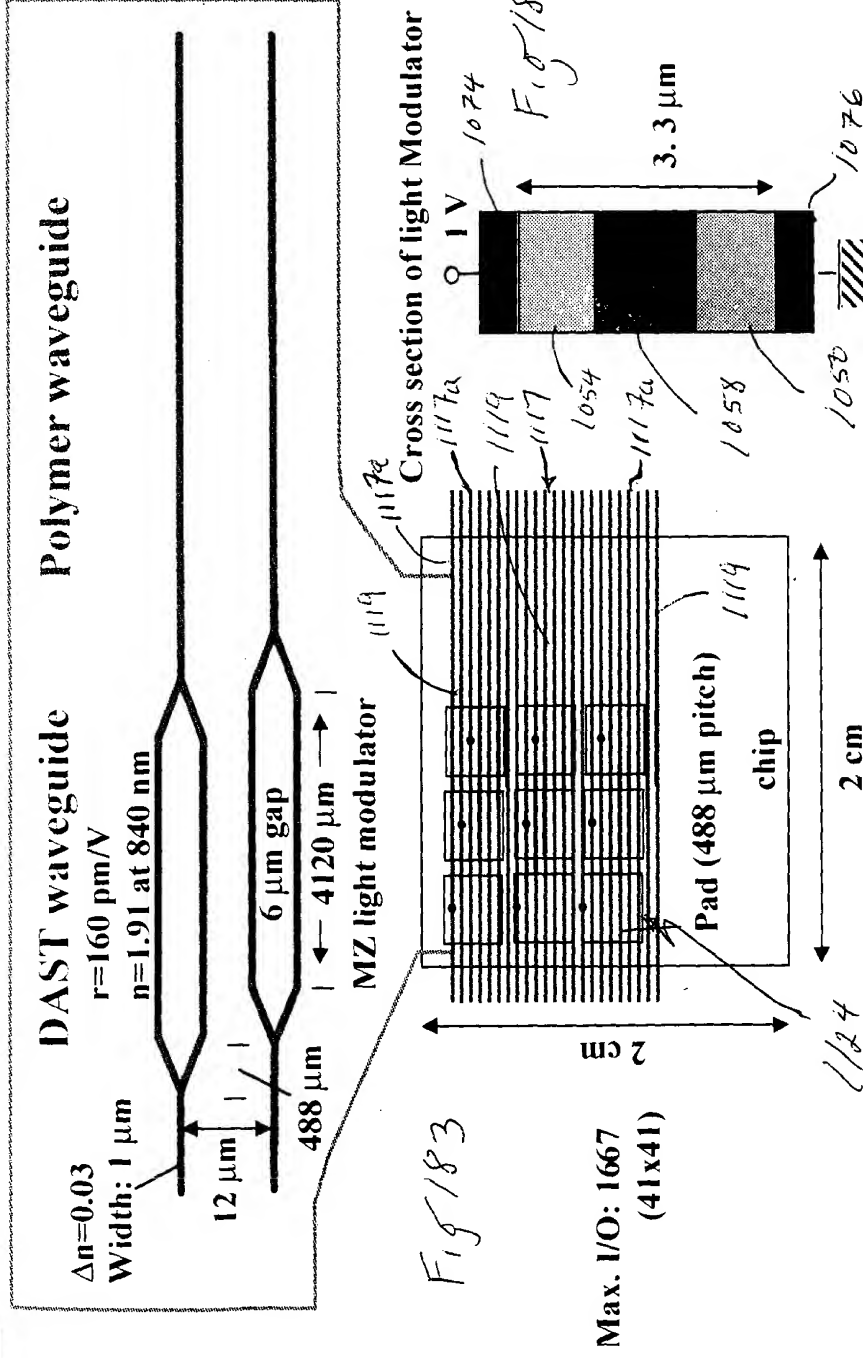
0076582-012201

# I/O Connection in OE Substrate (Planar Modulator)

Signal I/O count: 6000 =  $\lfloor 1500 \text{ I/O per Layer} \rfloor \times \lfloor 4\text{-Layer} \rfloor$



# I/O Connection in OE Substrate (Planar Modulator)



# I/O Connection in OE Substrate (OE-VLSI)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

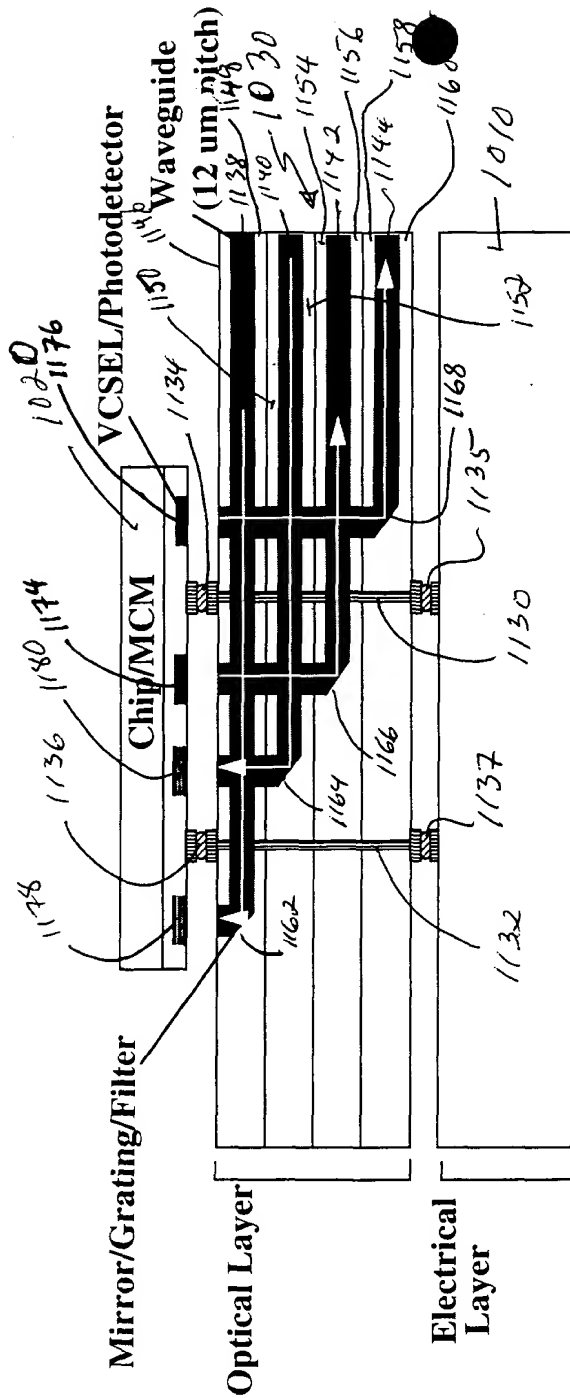


Fig 185

# I/O Connection in OE Substrate (OE-VLSI)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

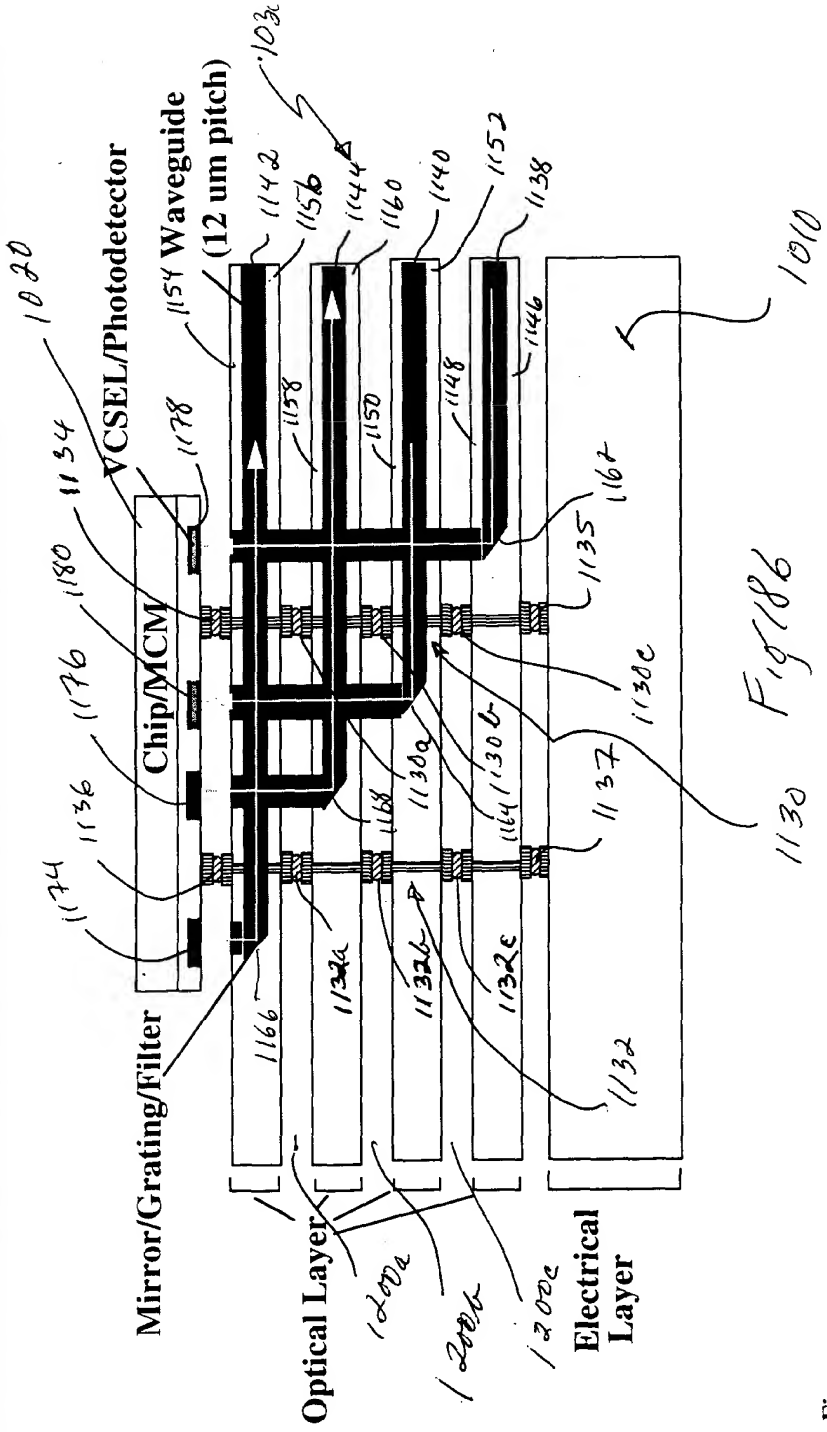
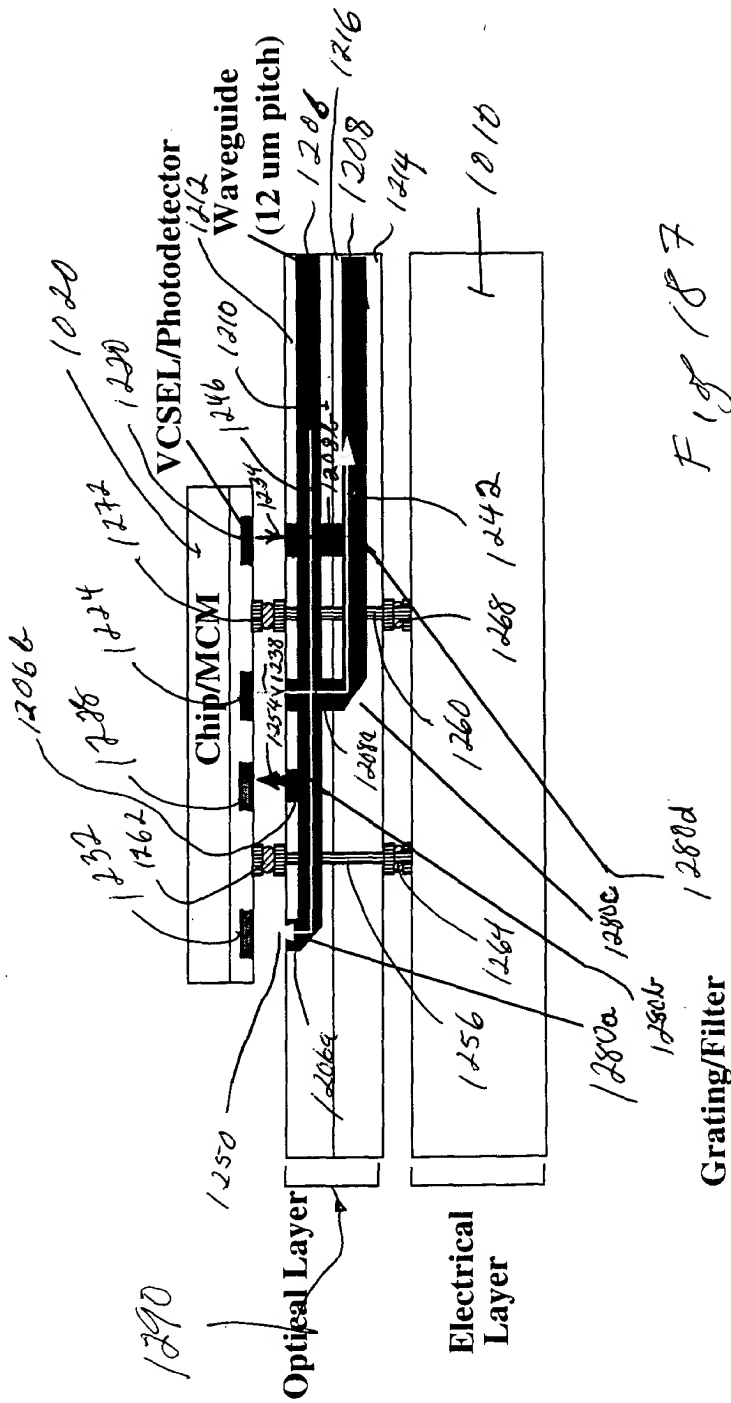


Fig.

## I/O Connection in OE Substrate (OE-VLSI, WDM)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

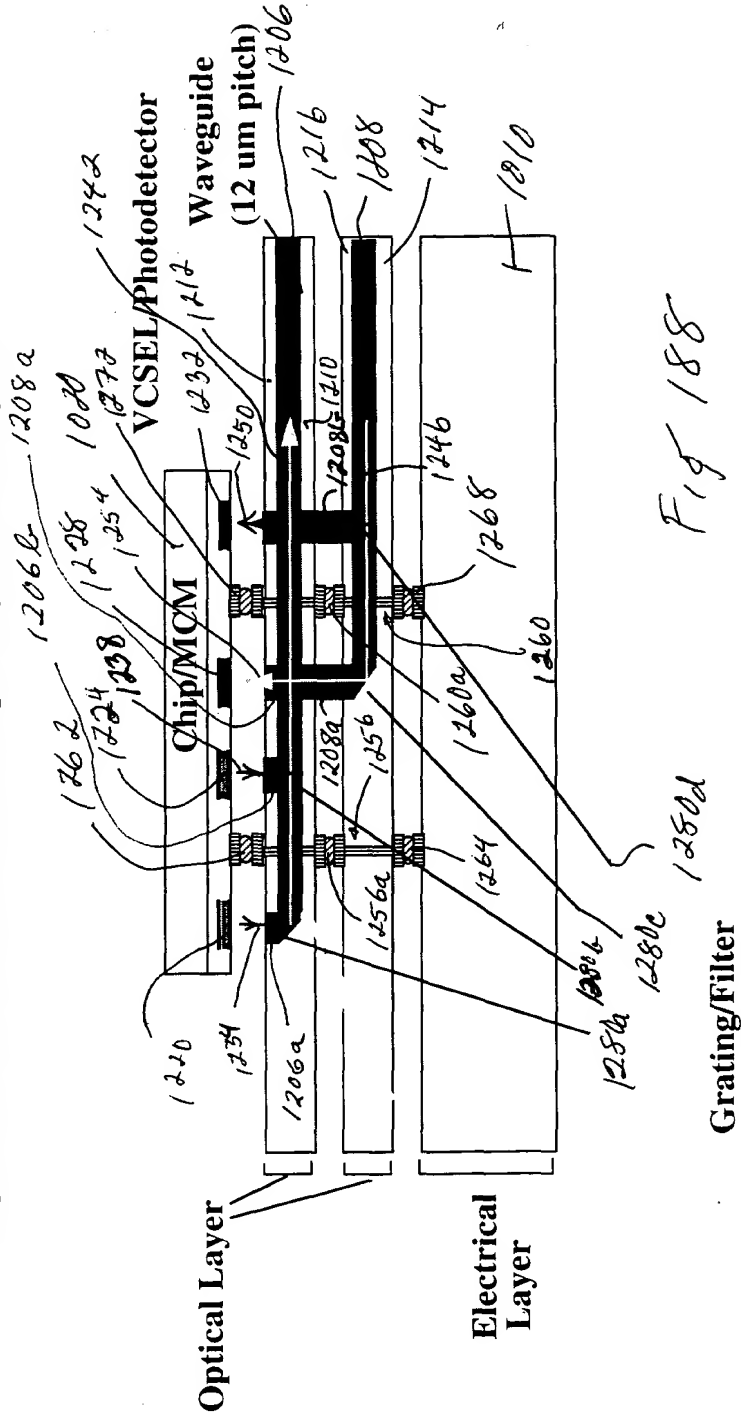


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## Grating/Filter

# I/O Connection in OE Substrate (OE-VLSI, WDM)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]





# I/O Connection in OE Substrate (Active OE Layer)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

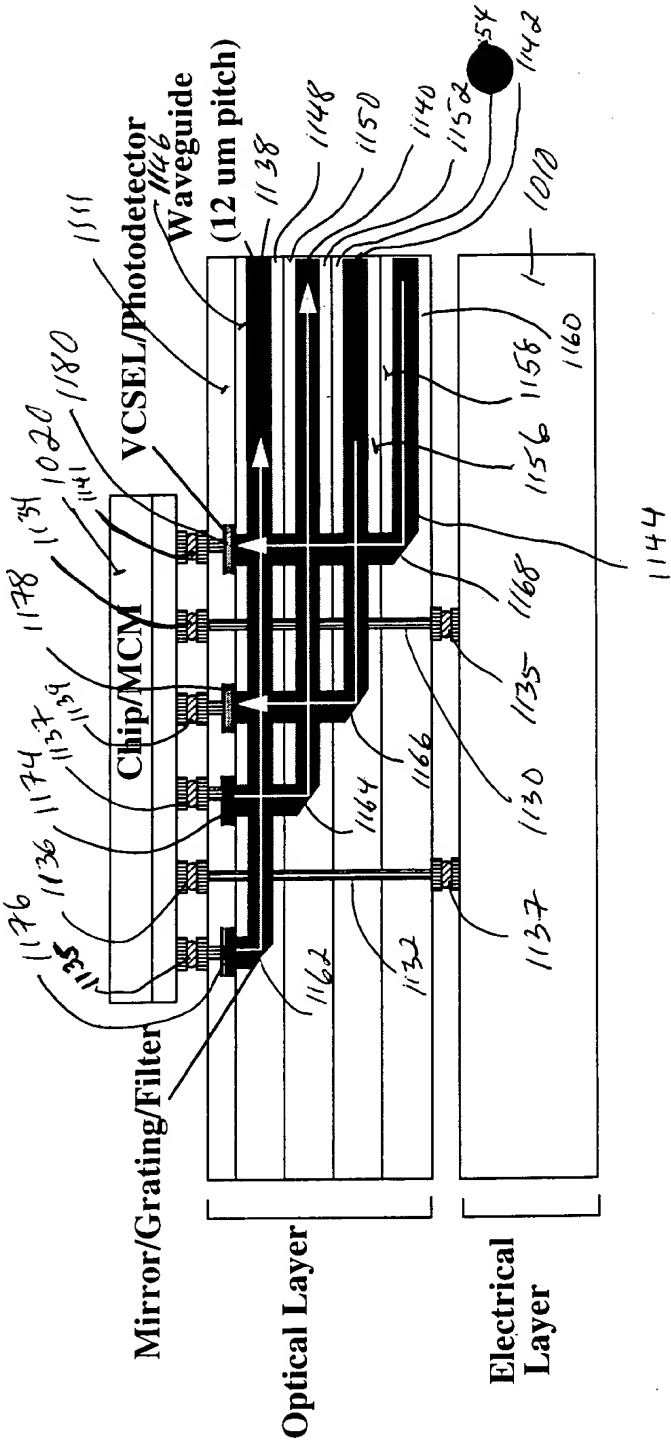


Fig. 189

# I/O Connection in OE Substrate (Active OE Layer)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

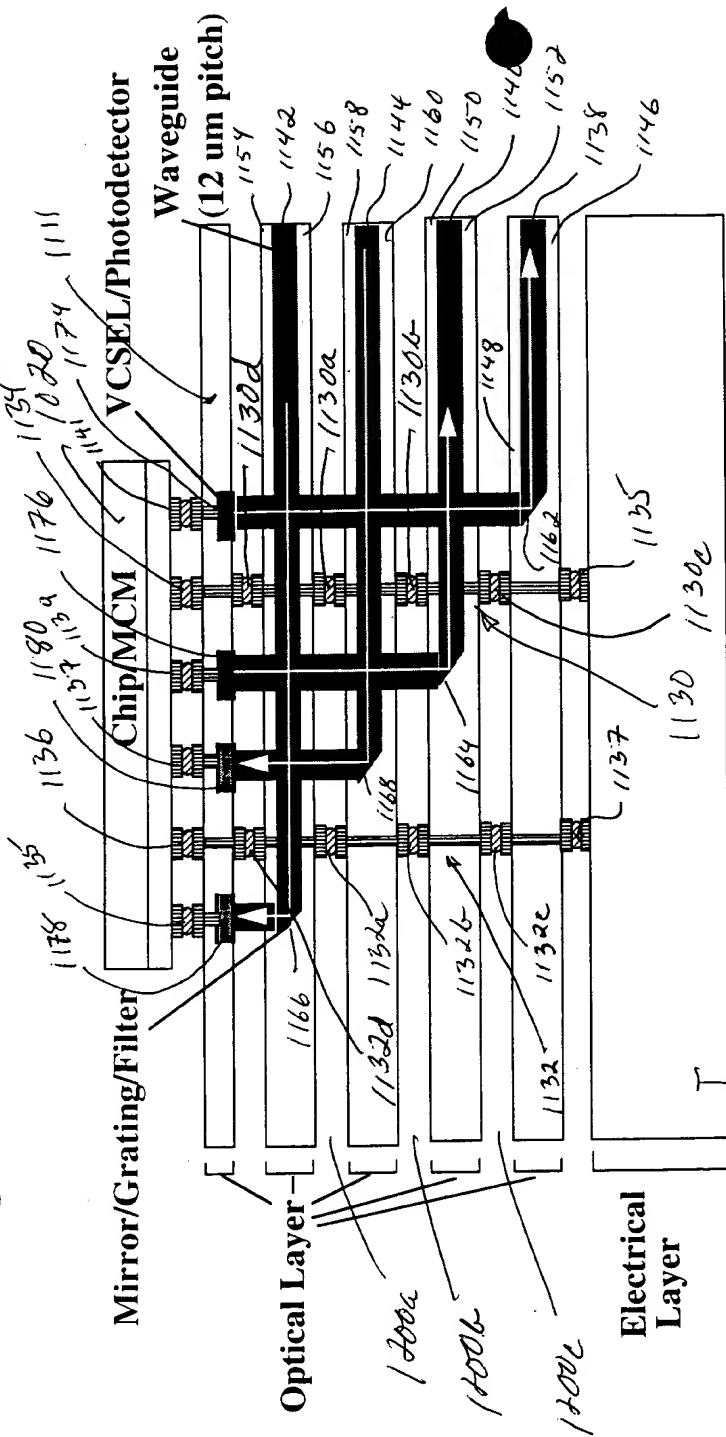


Fig. 9

Fig. 9

# I/O Connection in OE Substrate (Active OE Layer, WDM)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

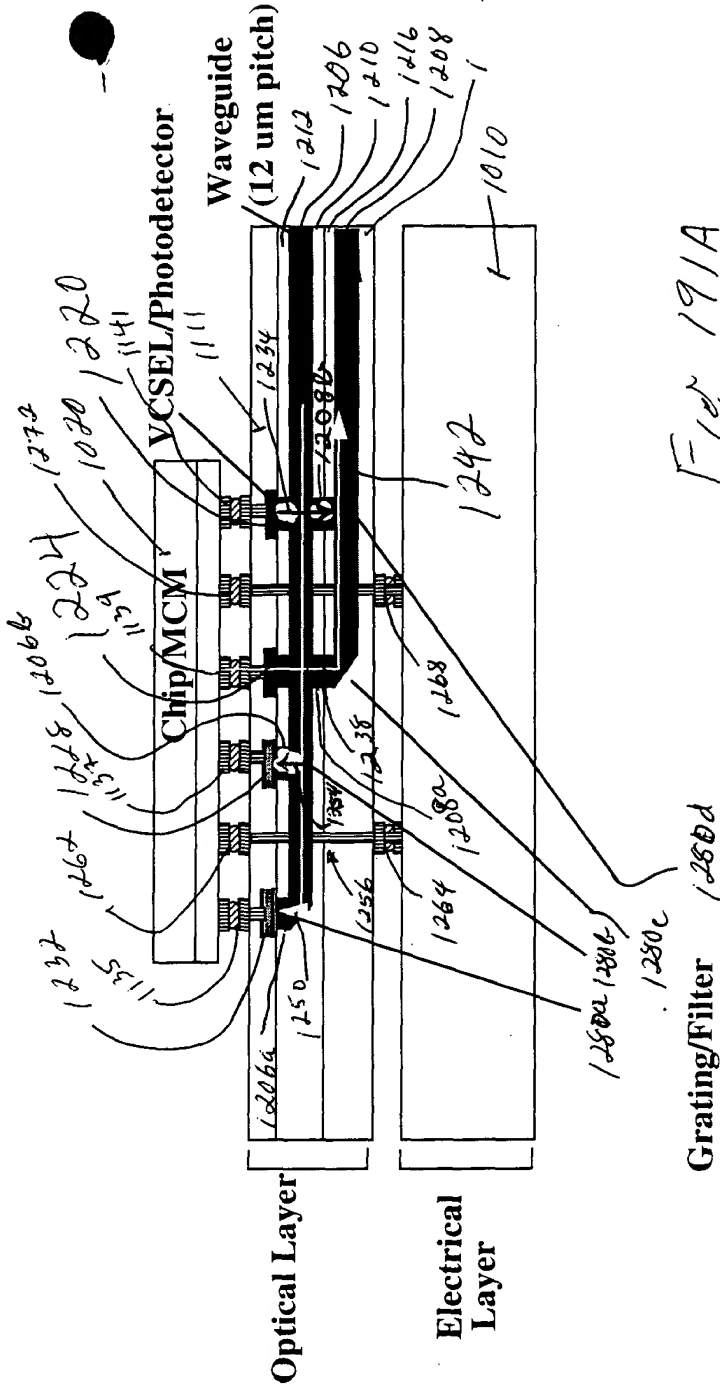


Fig. 10

# I/O Connection in OE Substrate (Active OE Layer, WDM)

Signal I/O count:  $6000 = [1500 \text{ I/O per Layer}] \times [4\text{-Layer}]$

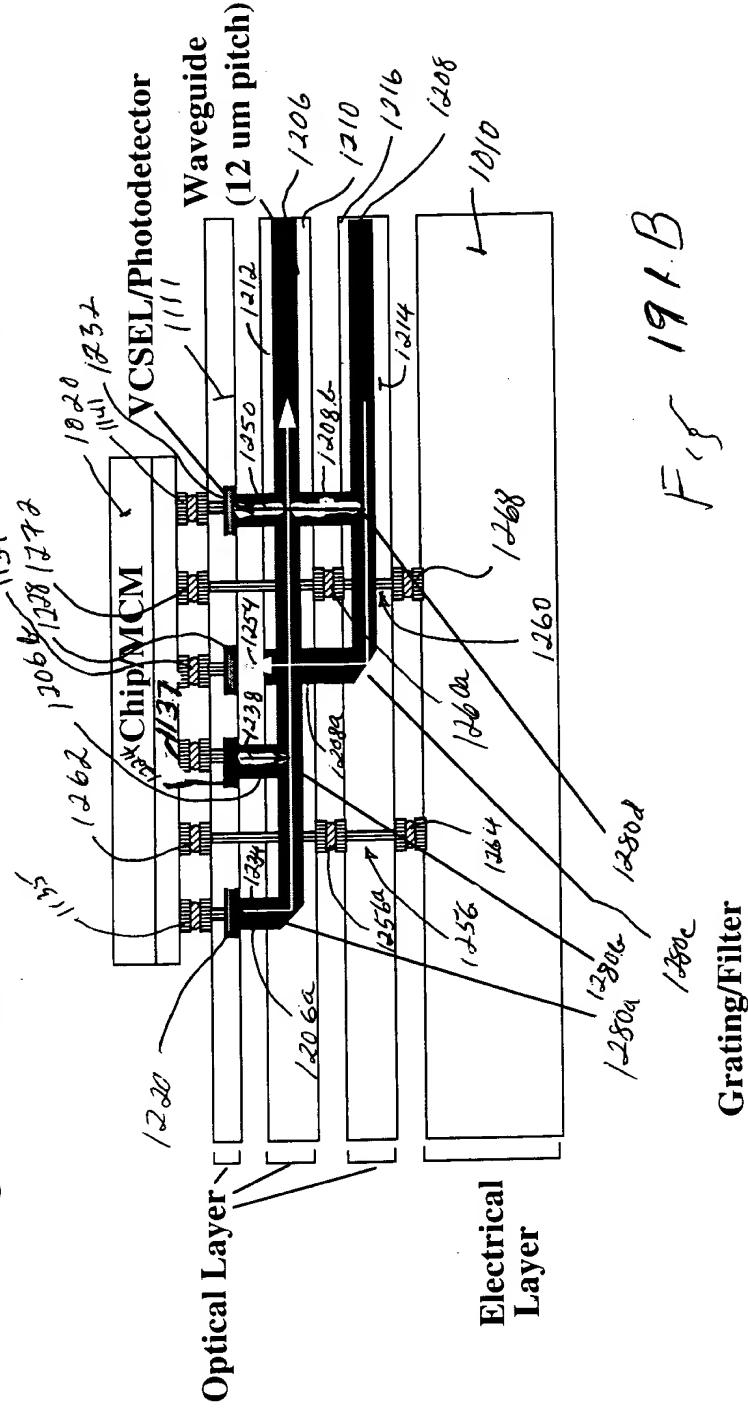
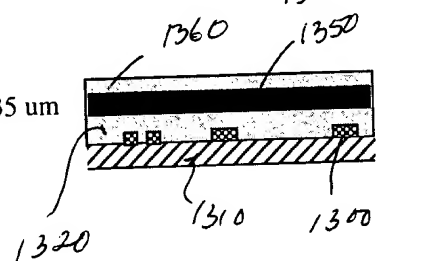
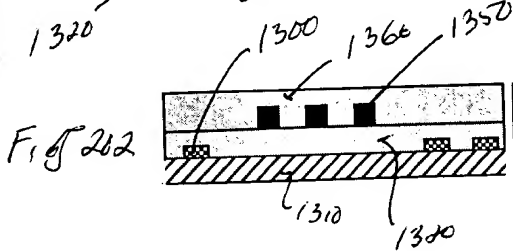
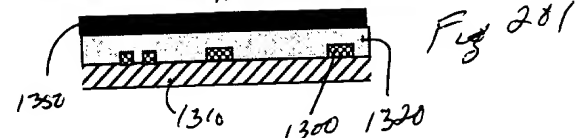
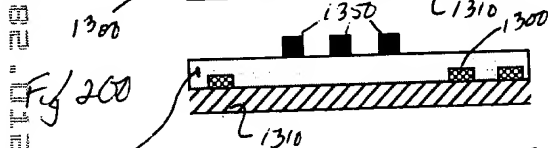
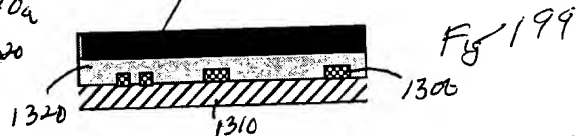
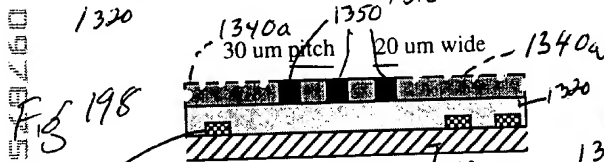
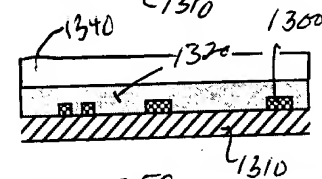
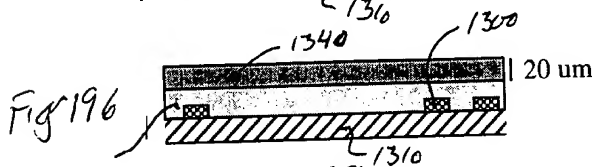
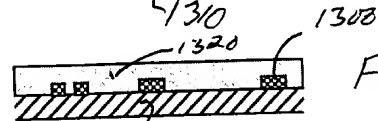
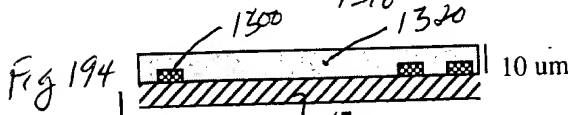
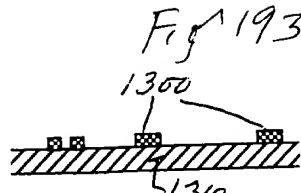
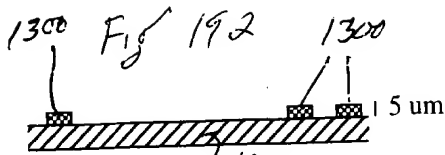
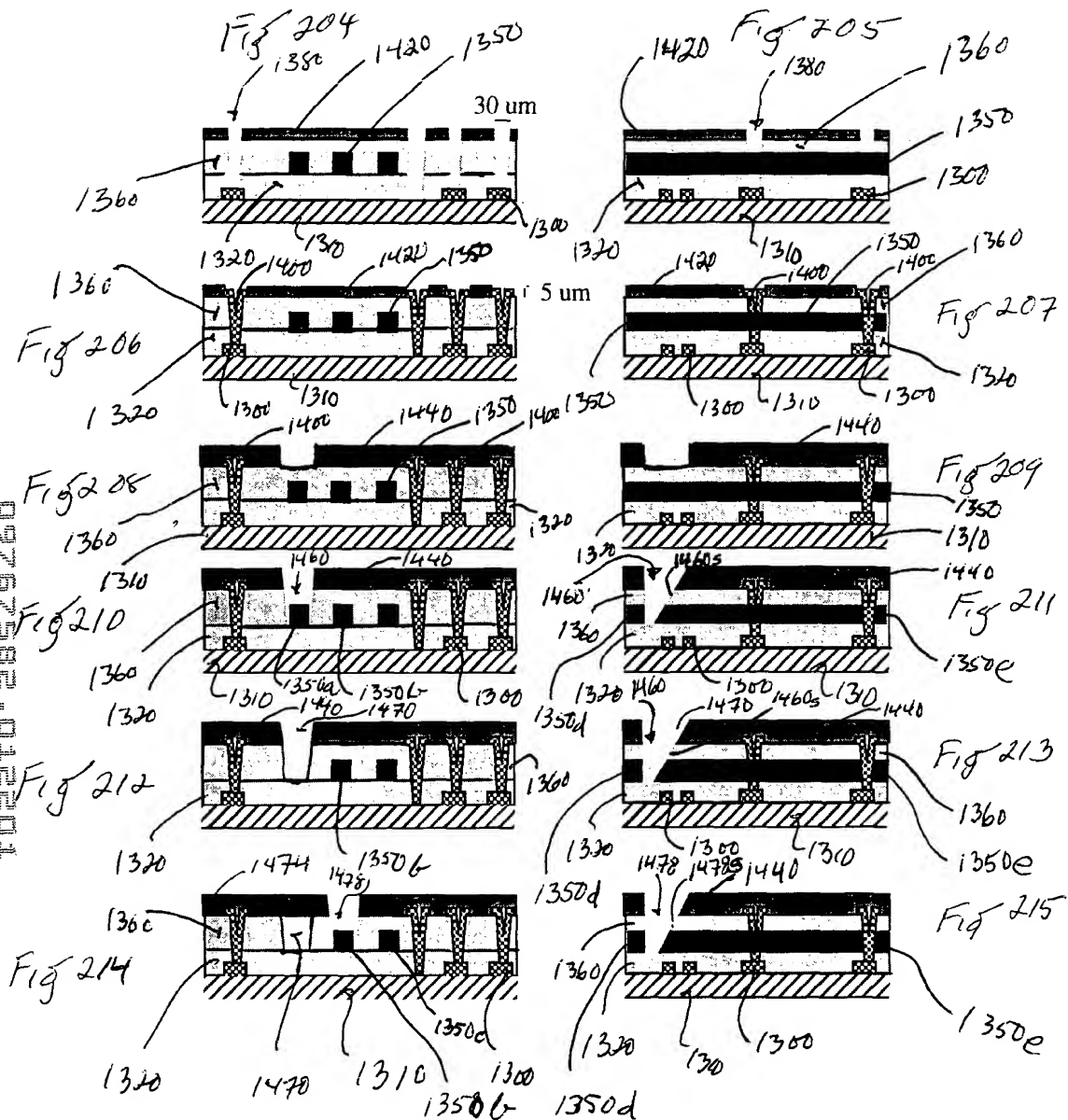


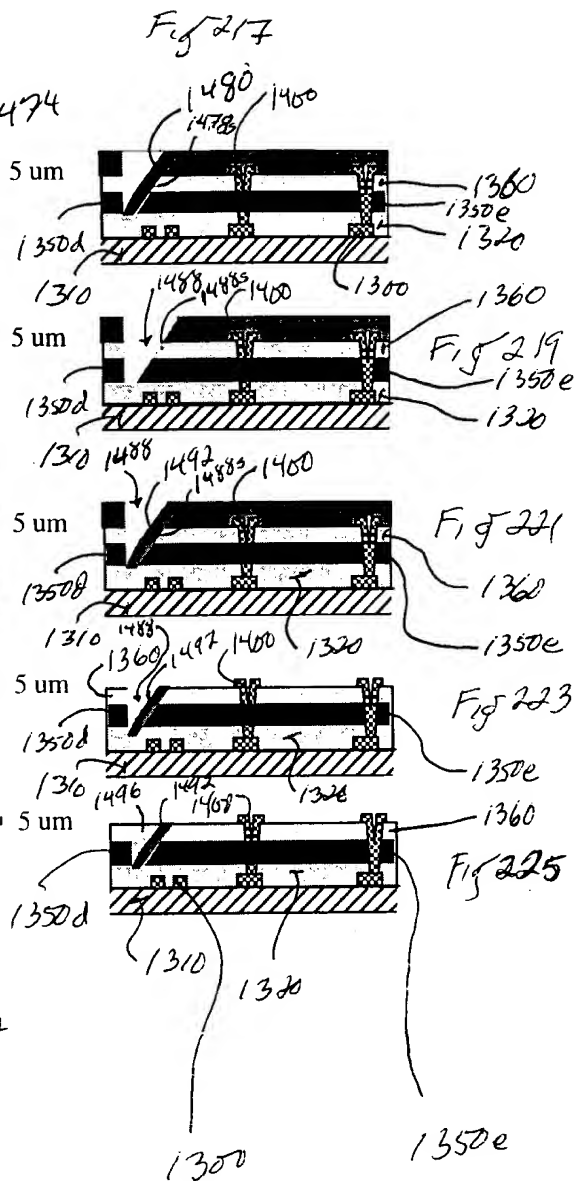
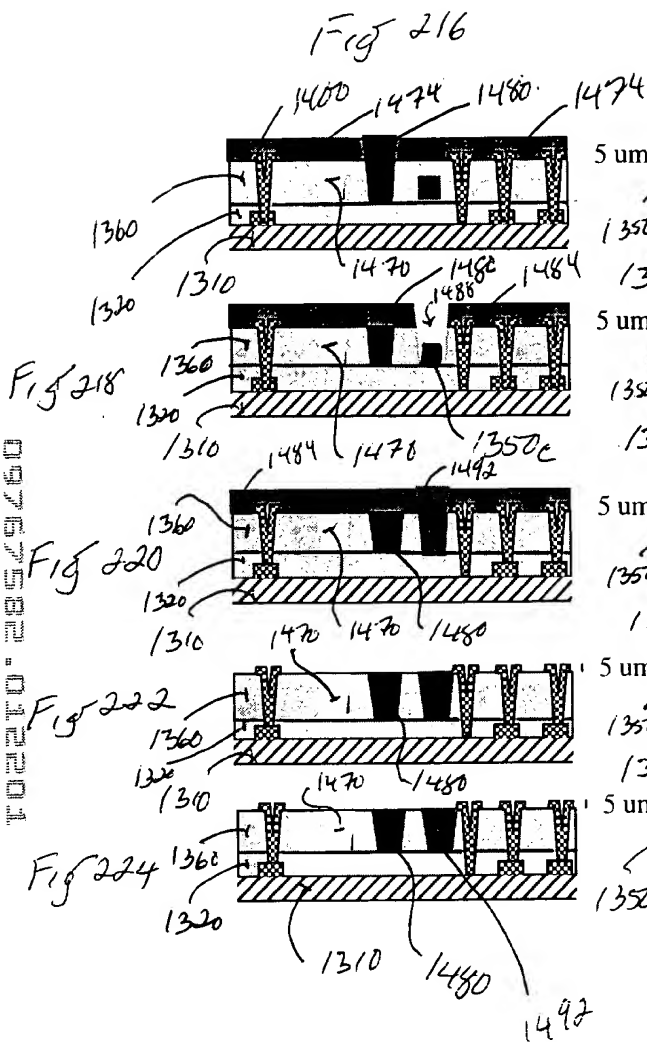
Fig. 11



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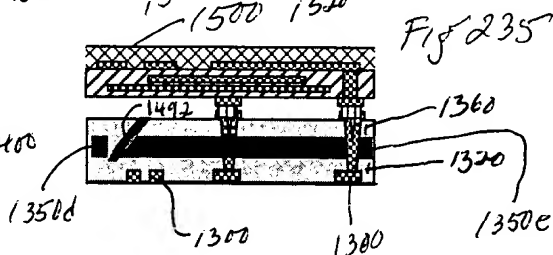
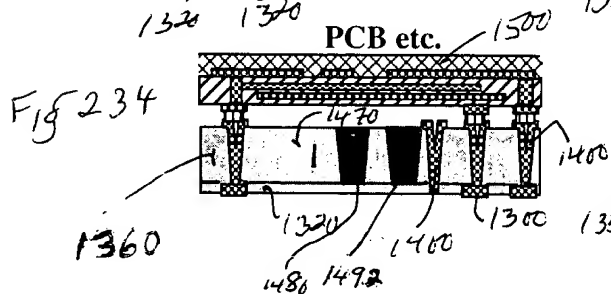
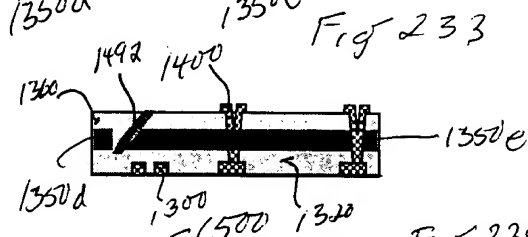
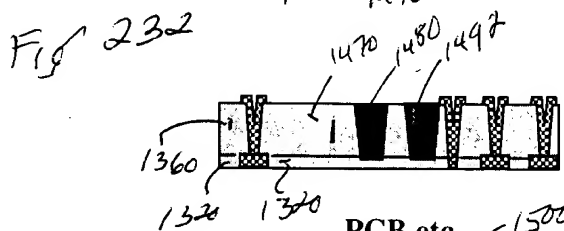
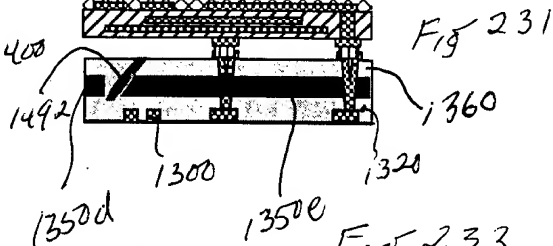
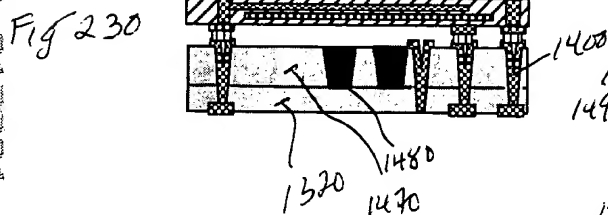
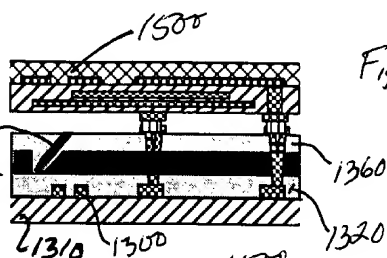
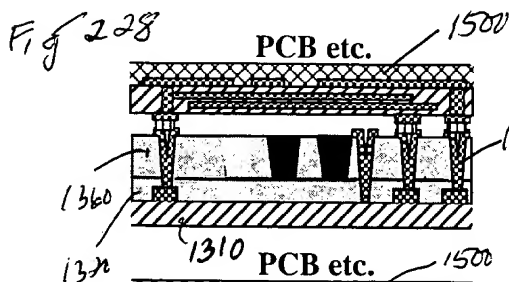
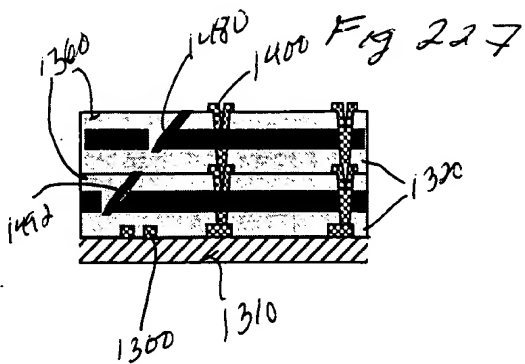
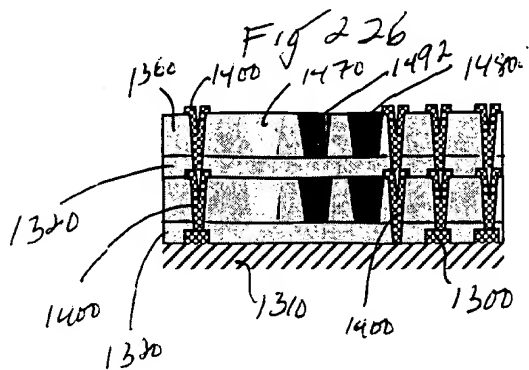




Fig 236

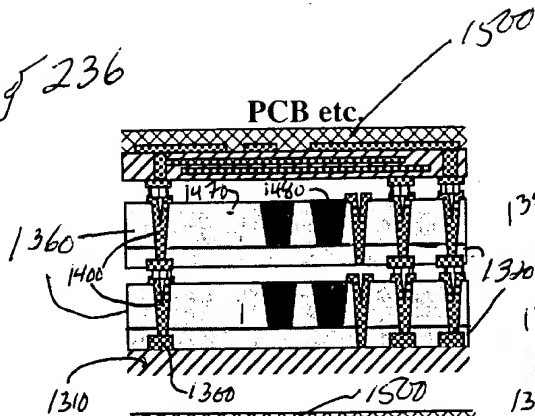


Fig 237

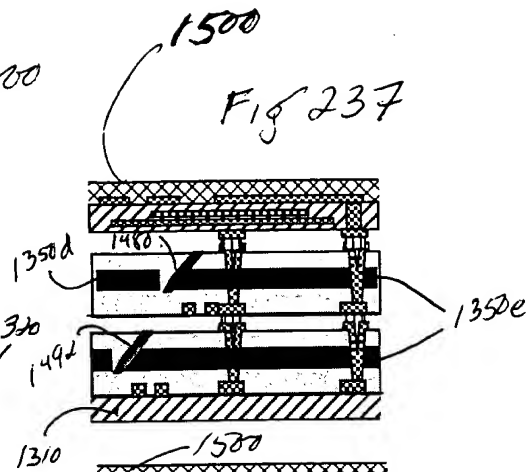


Fig 238

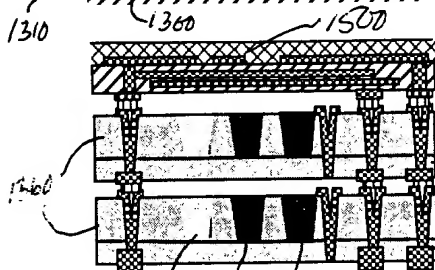


Fig 239

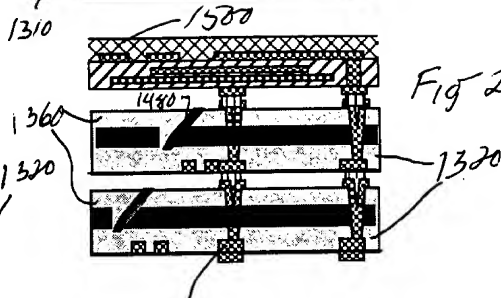


Fig 240

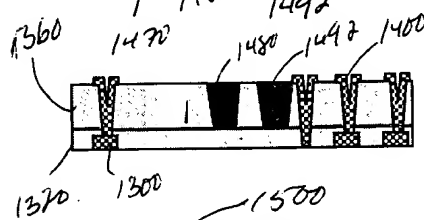


Fig 241

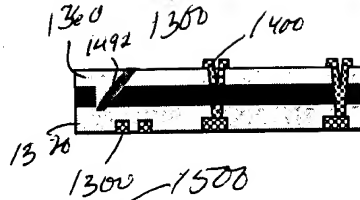


Fig 242

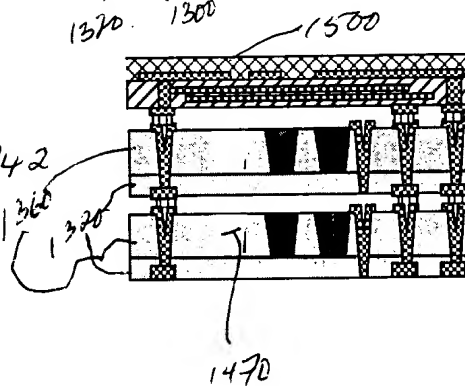
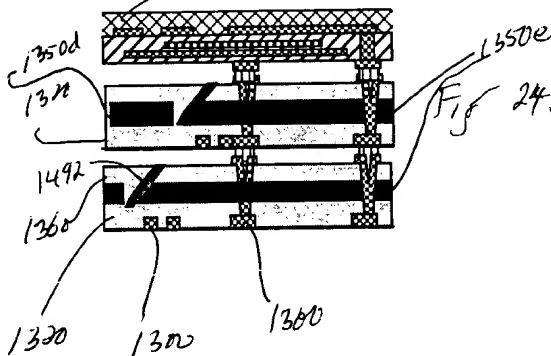


Fig 243



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Fig 244

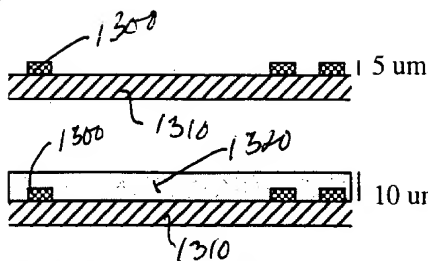


Fig 245

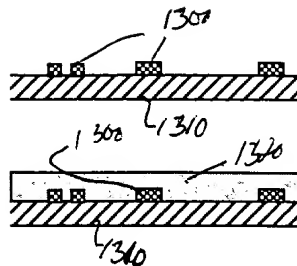


Fig 246

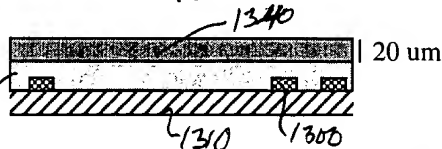


Fig 247

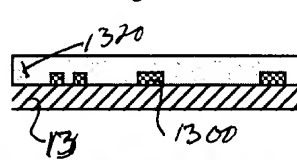


Fig 248

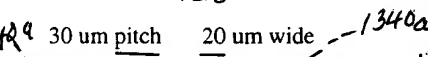


Fig 249

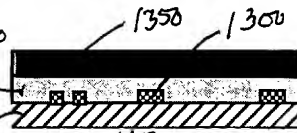


Fig 250



Fig 251

Fig 252

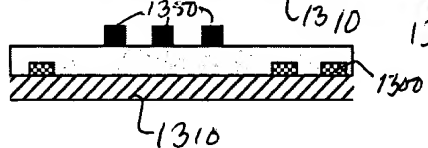


Fig 253

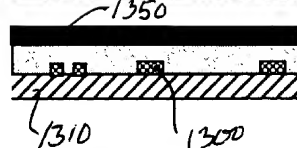


Fig 254

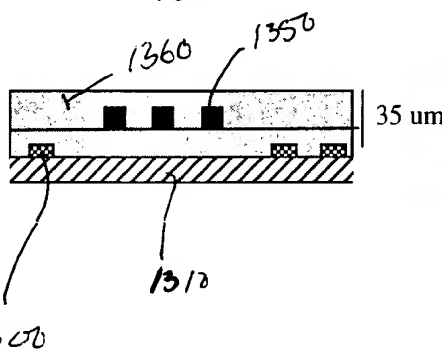
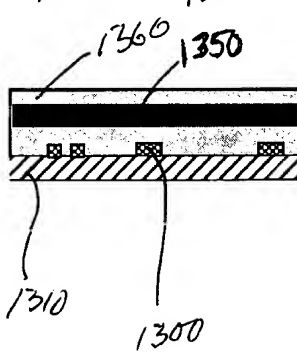


Fig 255



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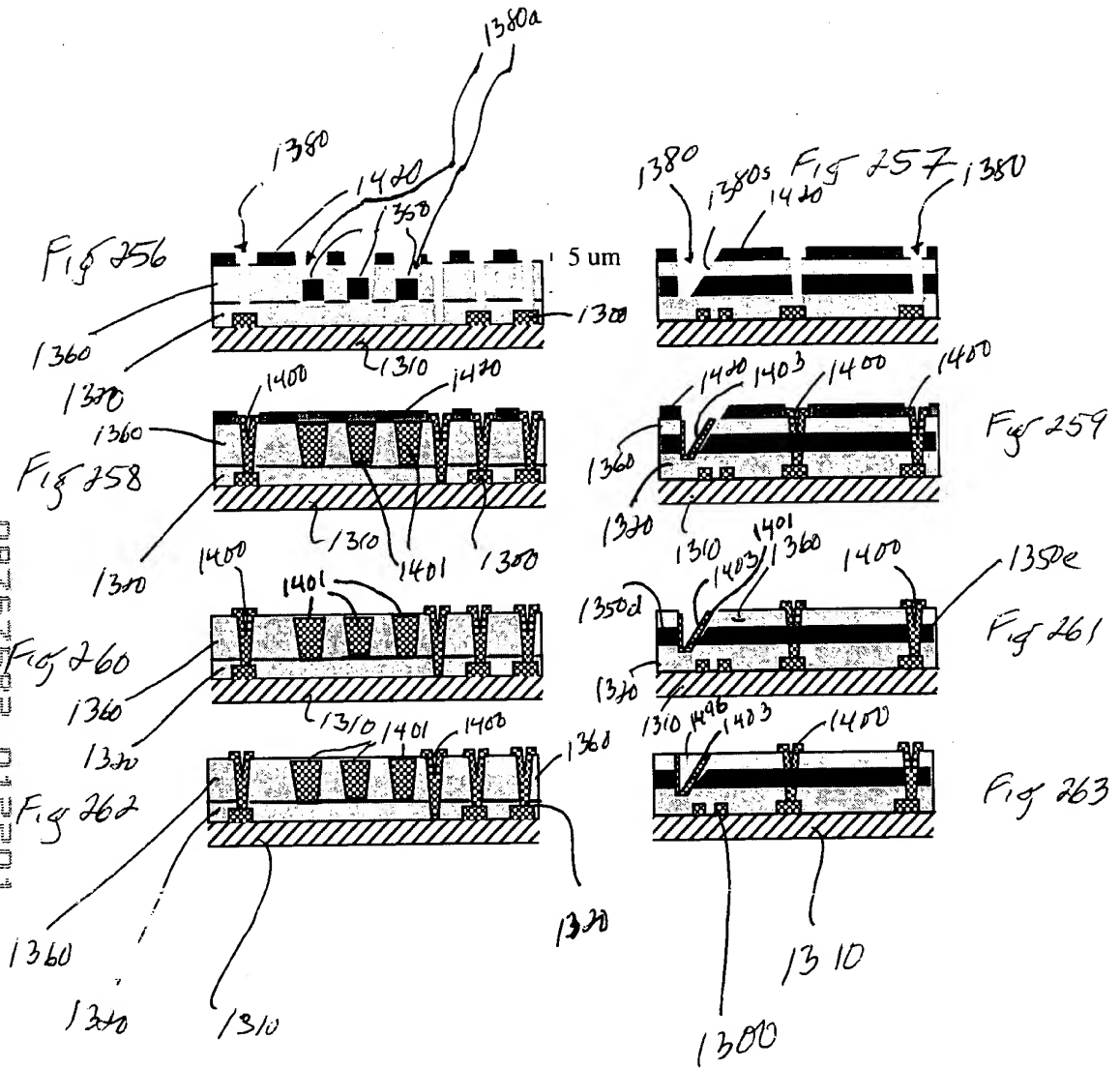


Fig 264

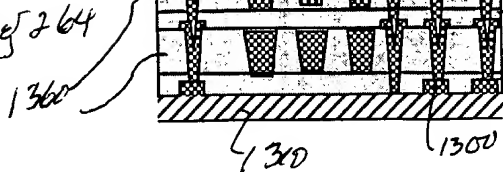


Fig 265

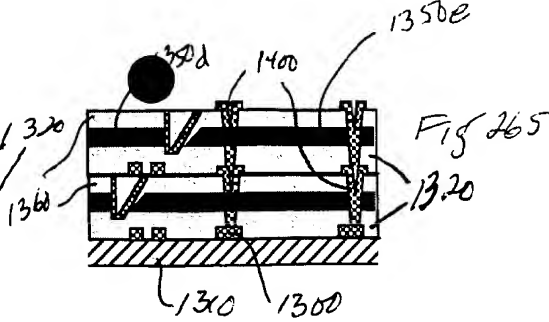


Fig 266

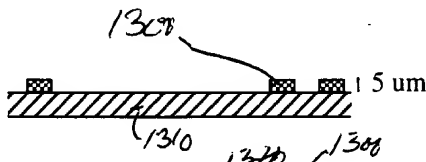


Fig 267

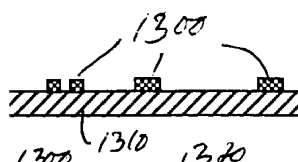


Fig 268



Fig 269

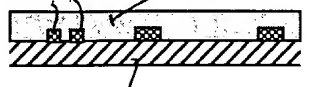


Fig 270

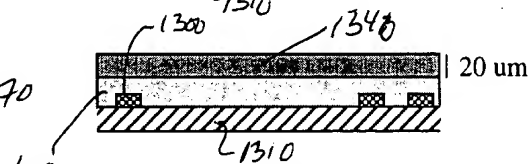


Fig 271

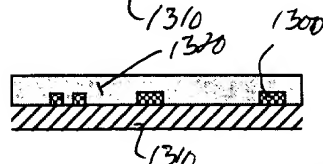


Fig 272

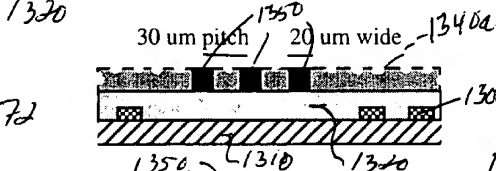


Fig 273

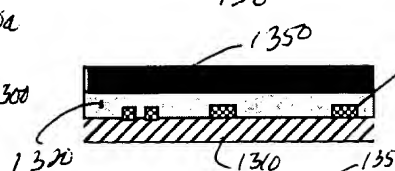


Fig 274

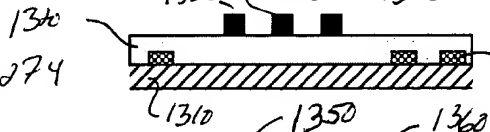


Fig 275

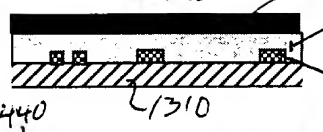


Fig 276

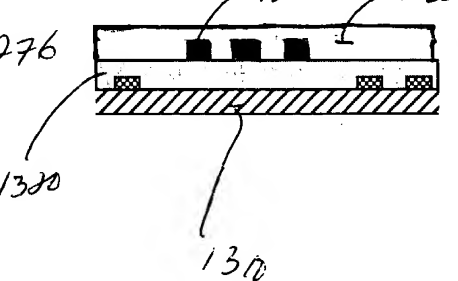
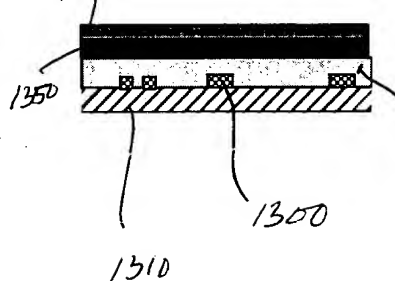
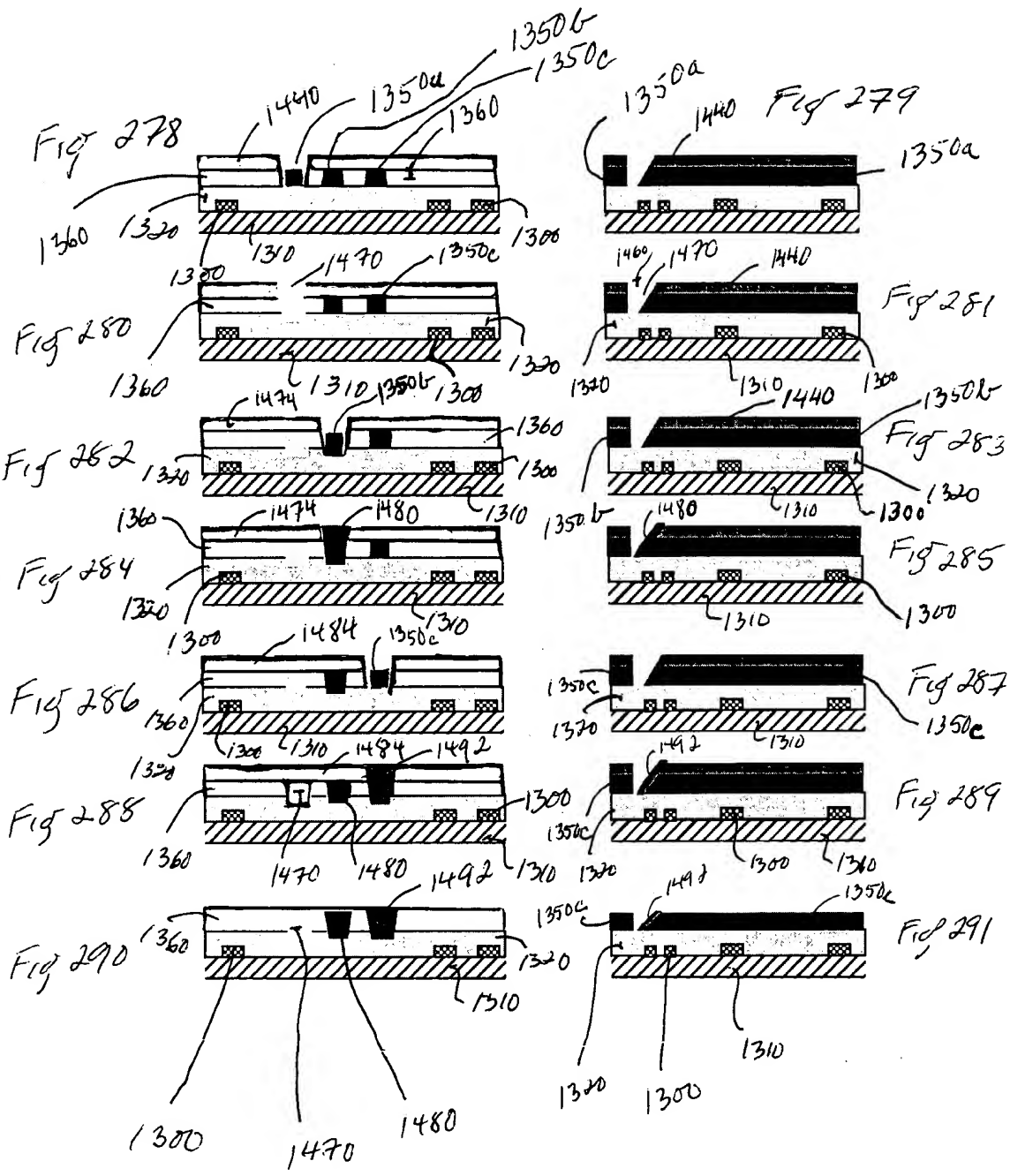
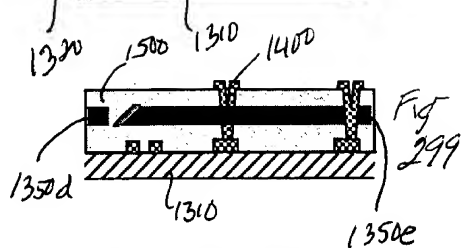
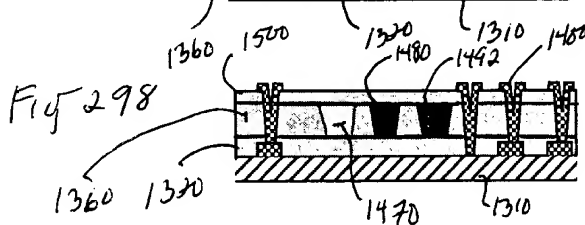
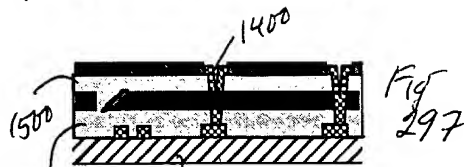
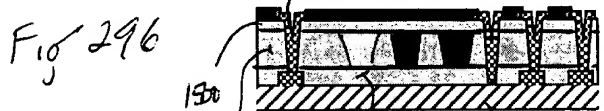
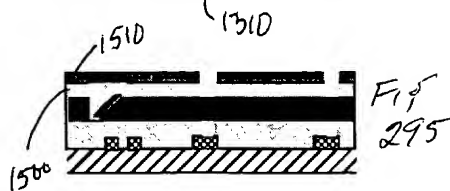
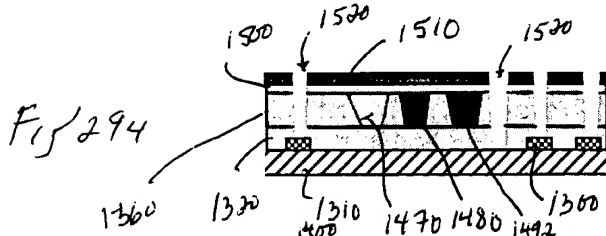
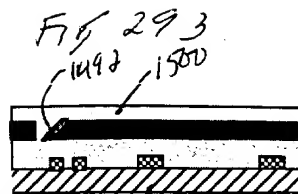


Fig 277

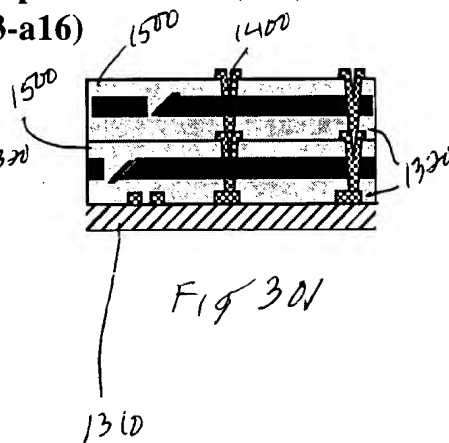
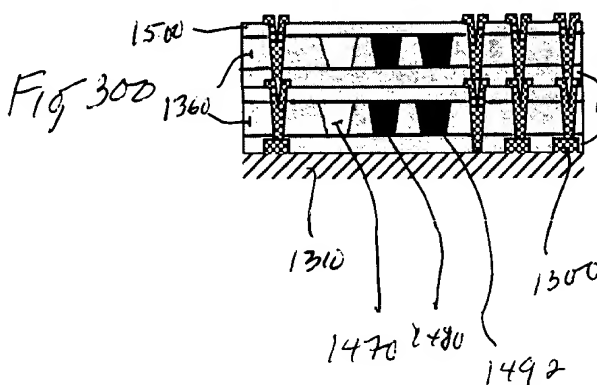


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**-it is also possible to repeat (a3-a16) or (a1, a3-a16)**



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Fig 302

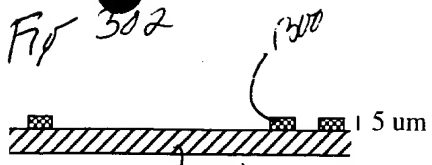


Fig 303

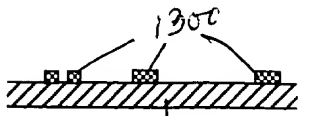


Fig 304

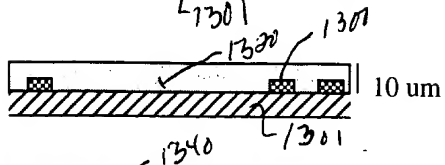


Fig 305

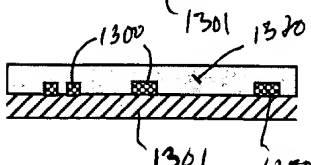


Fig 306

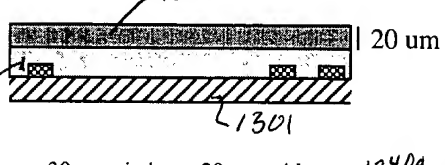


Fig 307

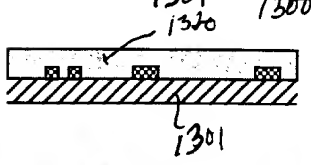


Fig 308

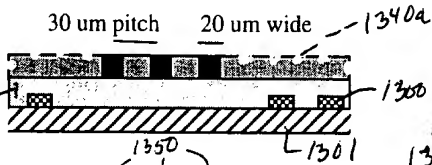


Fig 309

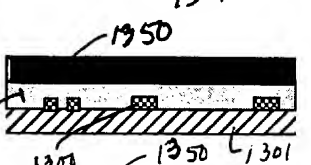


Fig 310

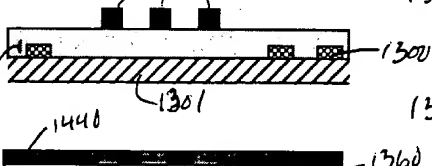


Fig 311

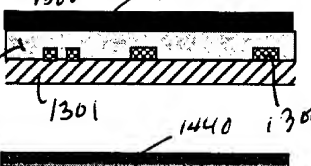


Fig 312

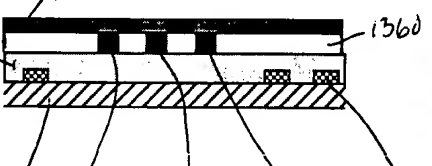
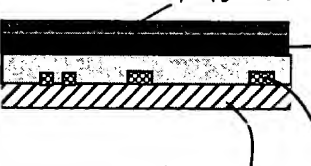


Fig 313



1301  
1350a  
1350b  
1350c  
1300

Fig 314

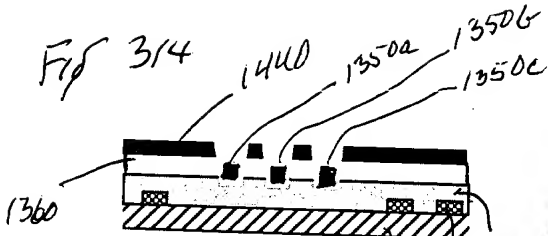


Fig 315

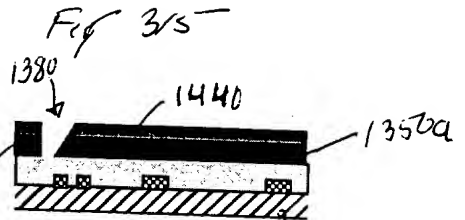


Fig 316

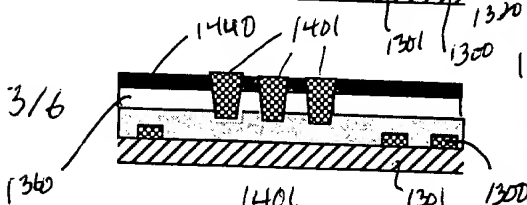


Fig 317

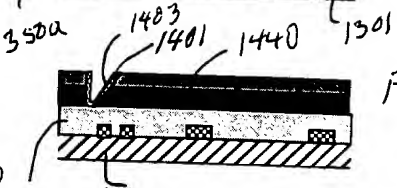


Fig 318

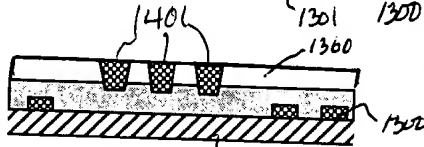


Fig 319



Fig 320

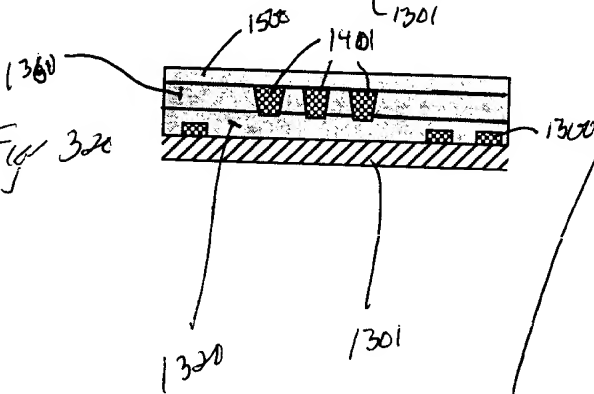
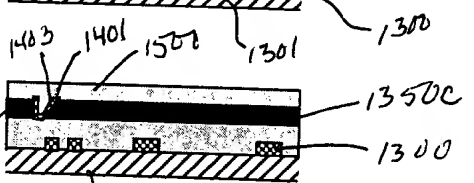
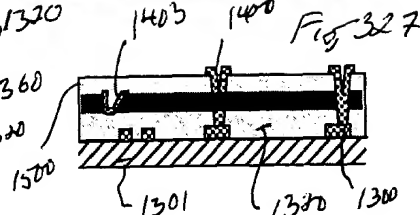
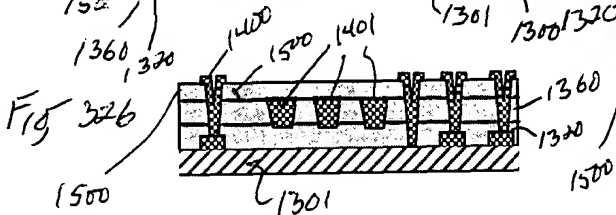
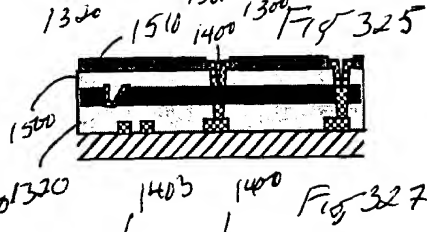
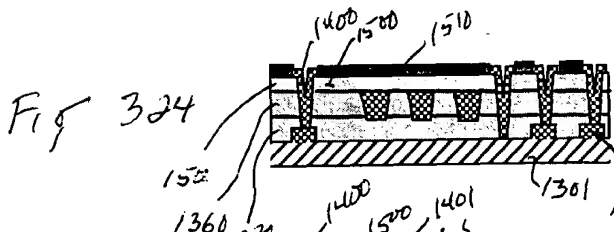
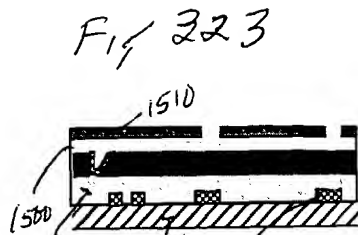
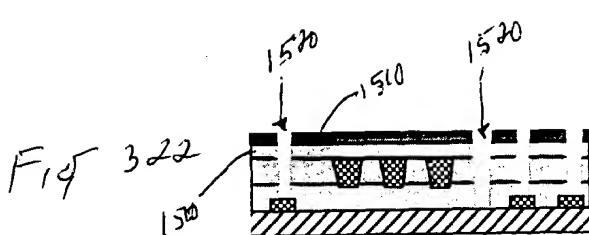


Fig 321

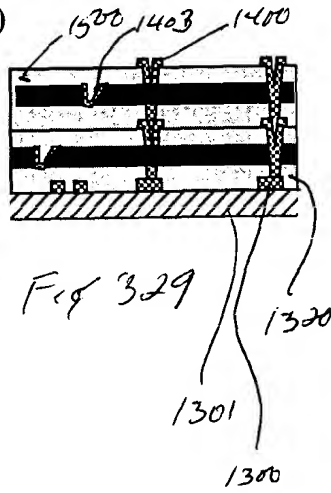
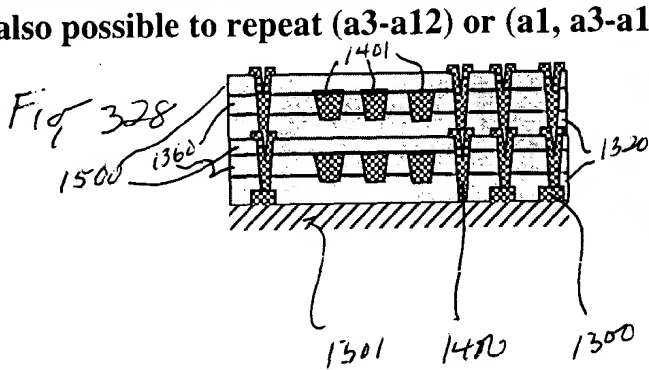


1350c

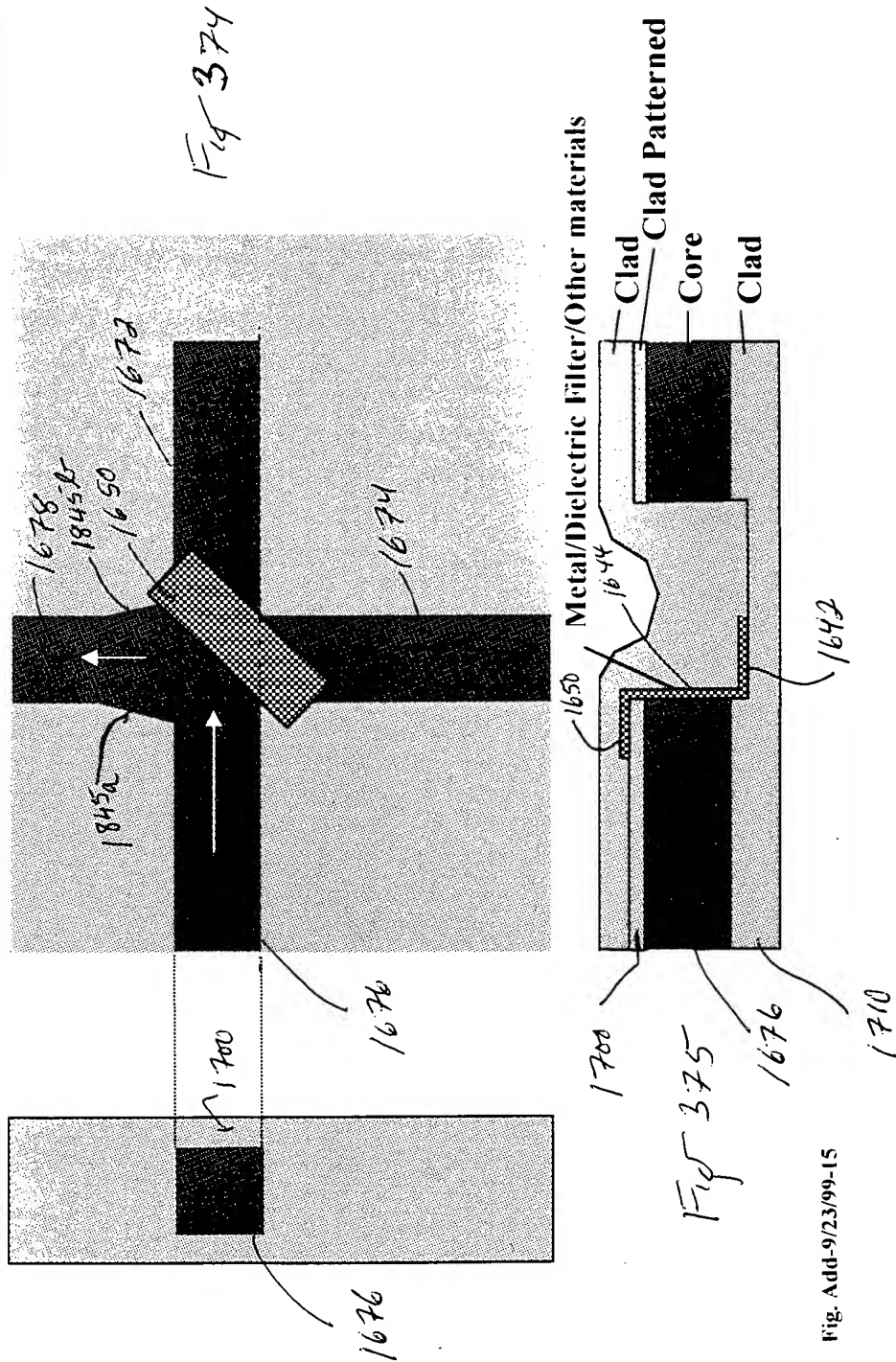




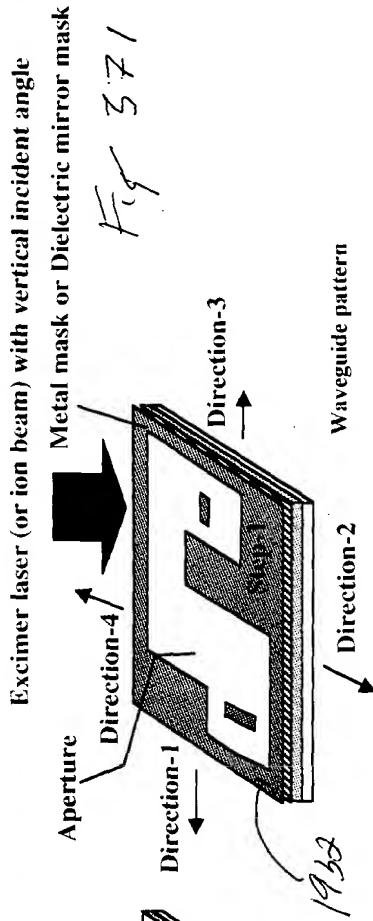
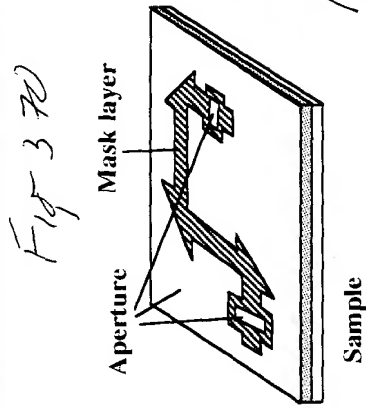
In the case of multi layer (a1-a12) process is repeated on the (a12).  
-it is also possible to repeat (a3-a12) or (a1, a3-a12)



## Invented Corner Turning Structure (A)



# MNA, MNE Example for Add2 example



Excimer laser (or ion beam) with tilted incident angle

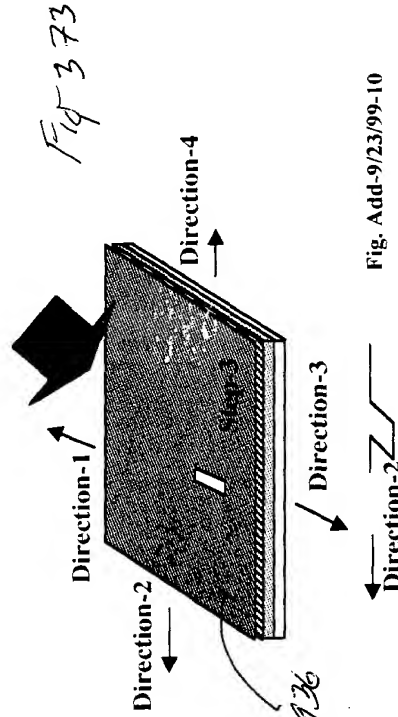
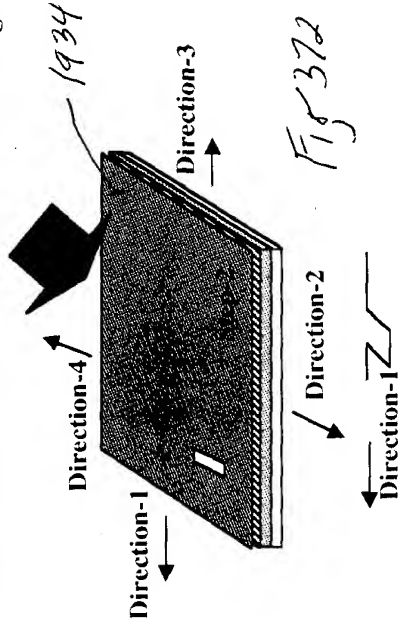
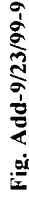


Fig. Add-9/23/99-10

File 352



## Excimer Laser Ablation Example for Beveled Cut (2)

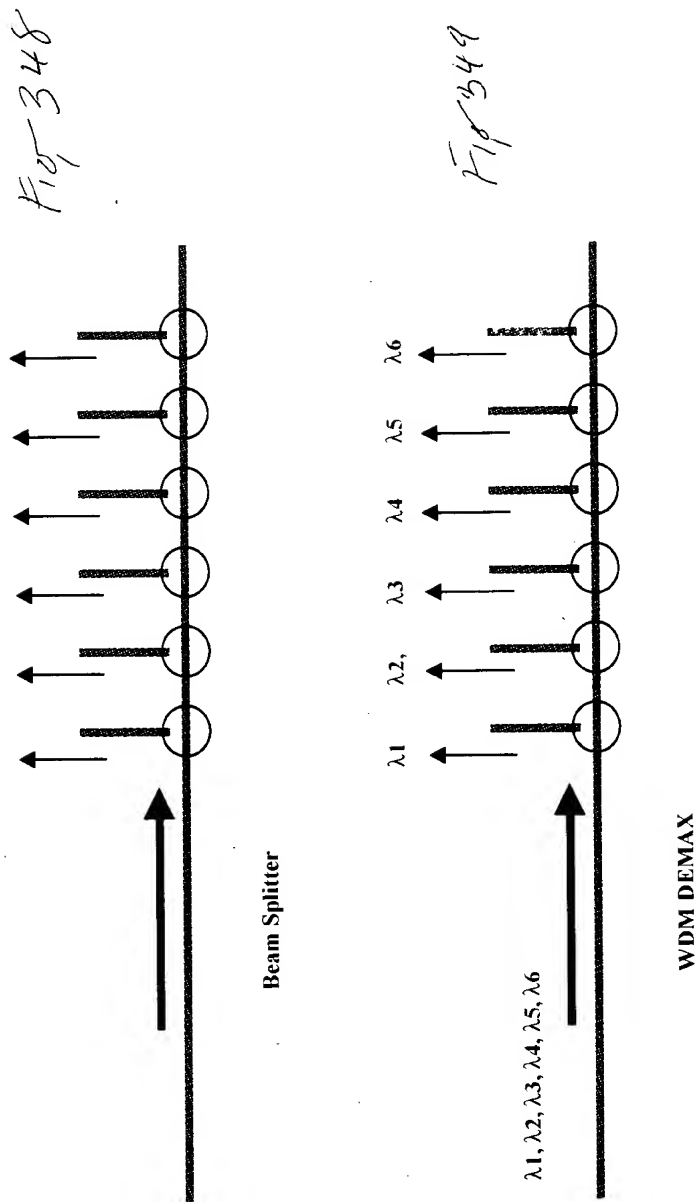


Fig. Add-9/23/99-8

# Invented Coupler Structure (II)

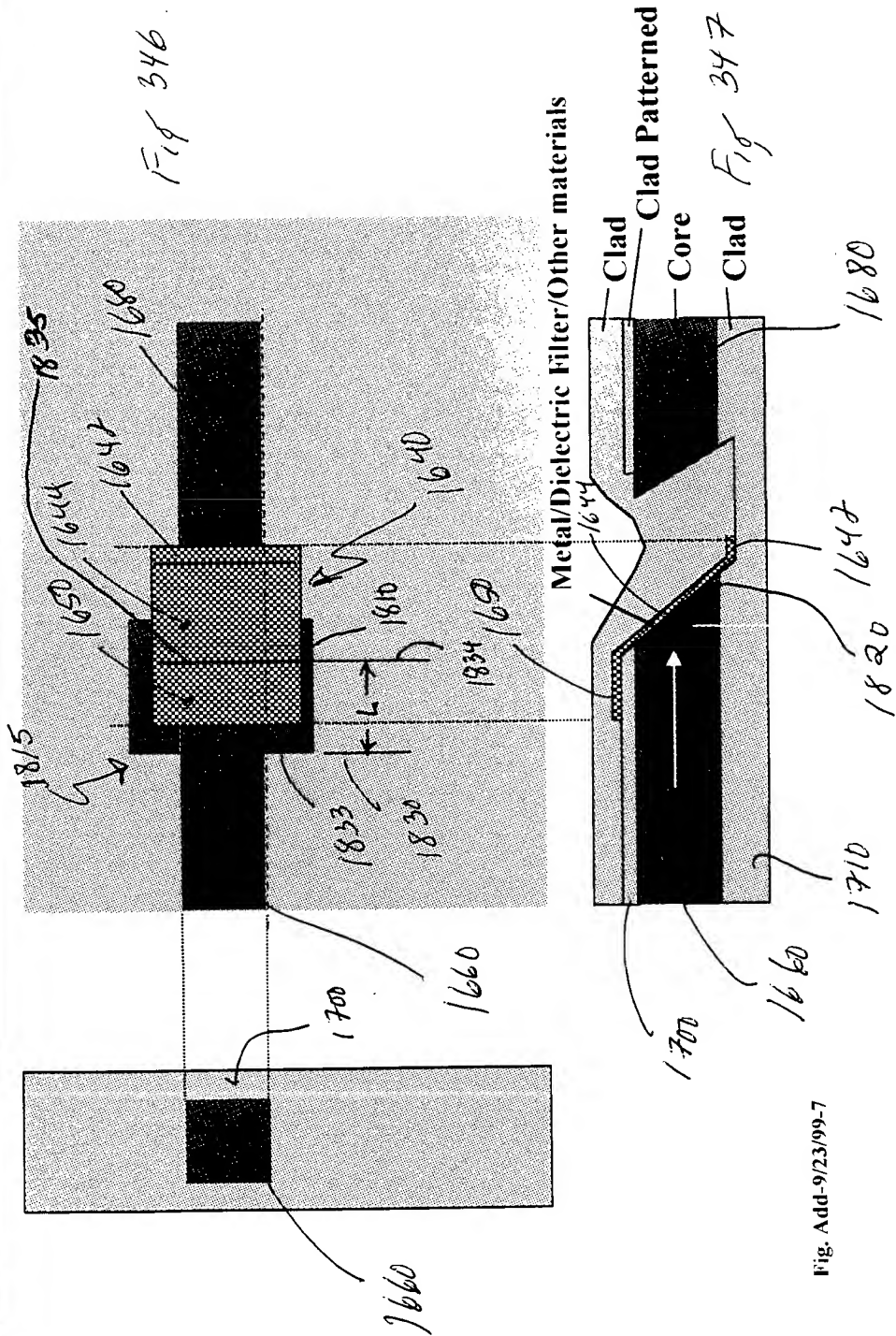
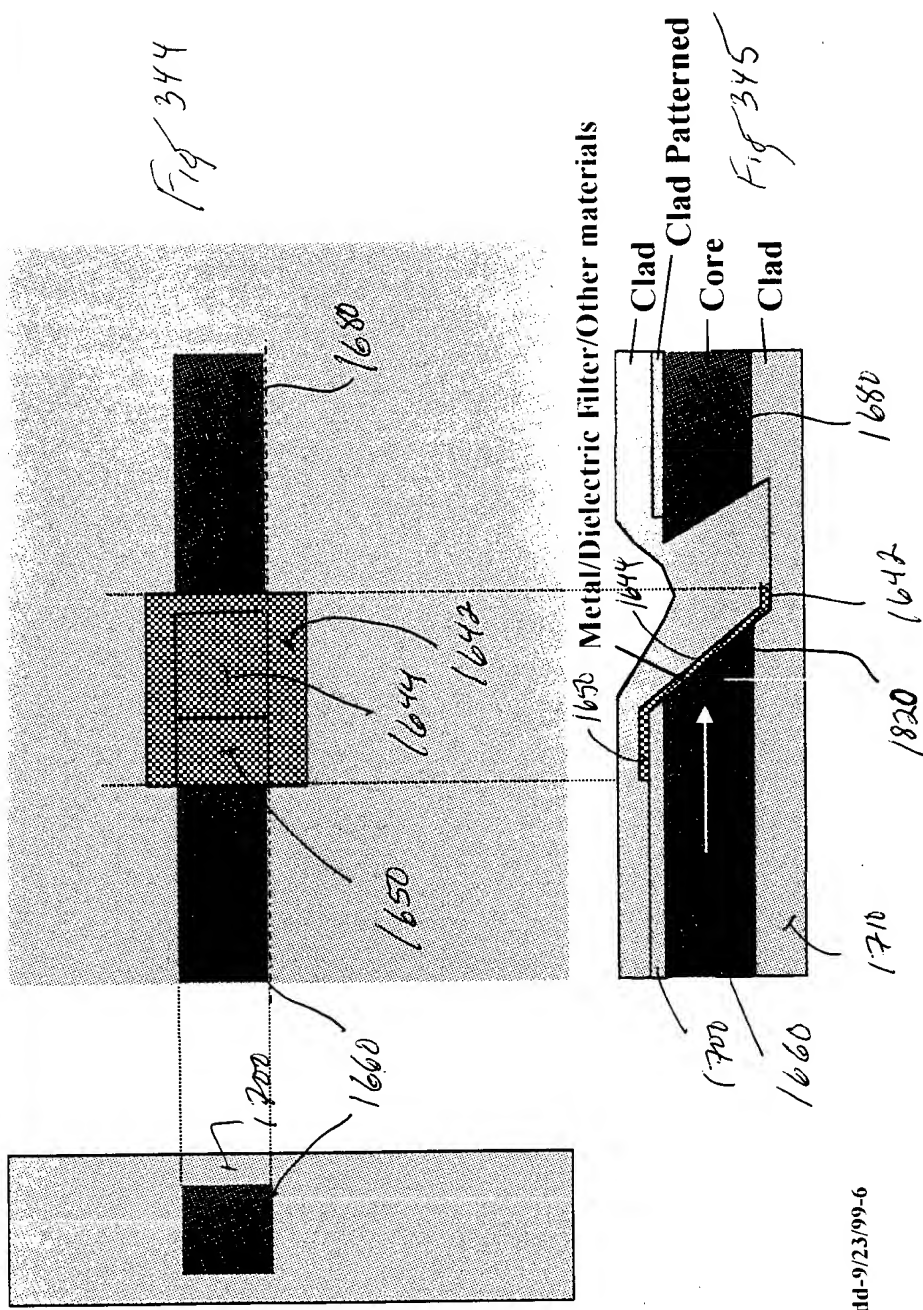


Fig. Add-9/23/99-7

# Invented Coupler Structure (I)



**Fig. Add-9/23/99-6**

# Conventional Coupler Structure (I)

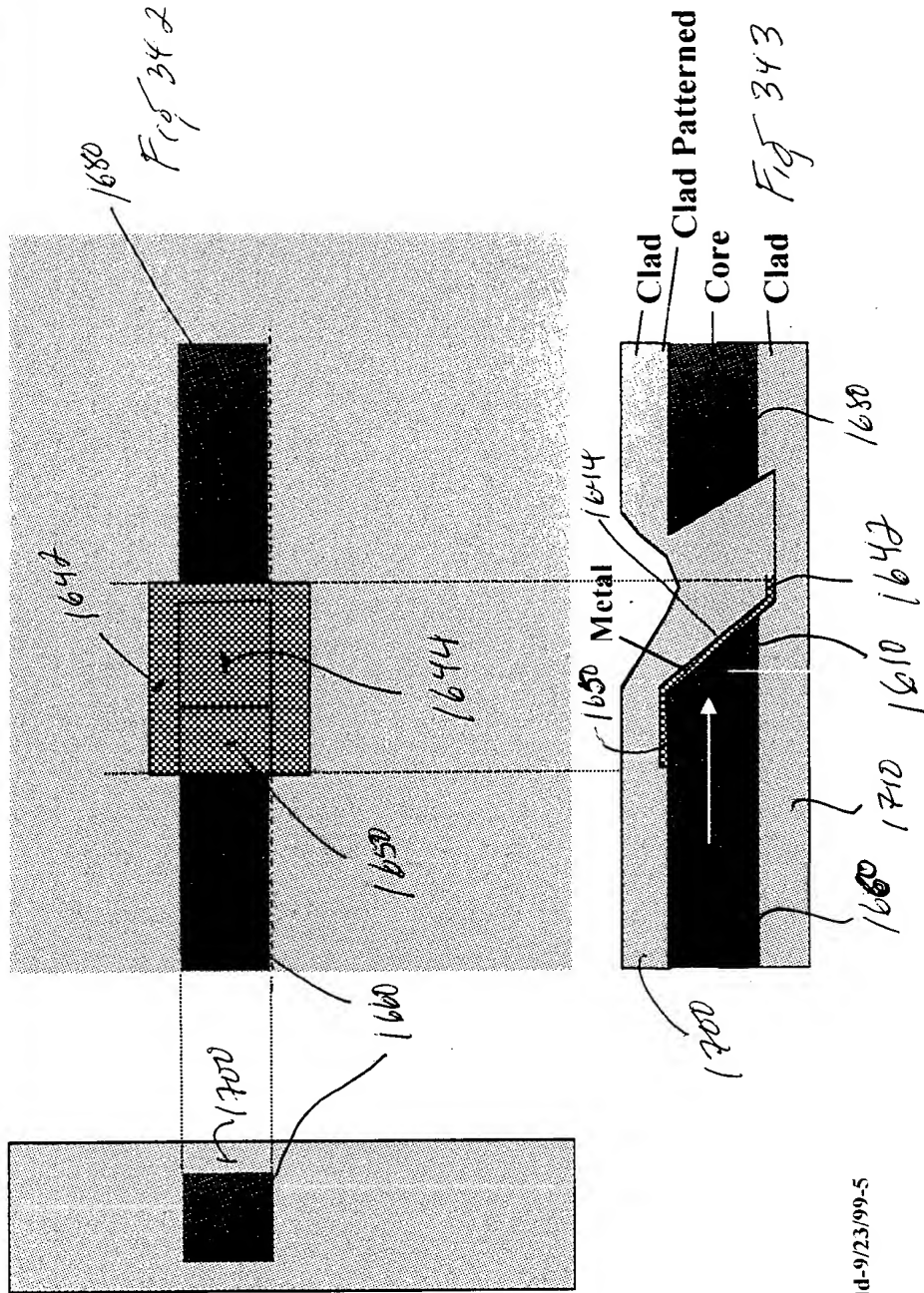


Fig. Add-9/23/99-5



Fig 340

Fig-341

# Invented Corner Turning Structure (I)

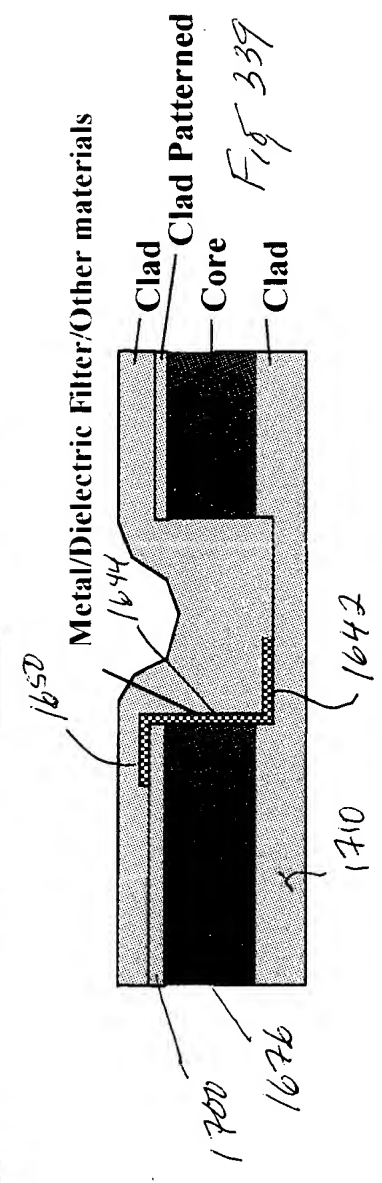
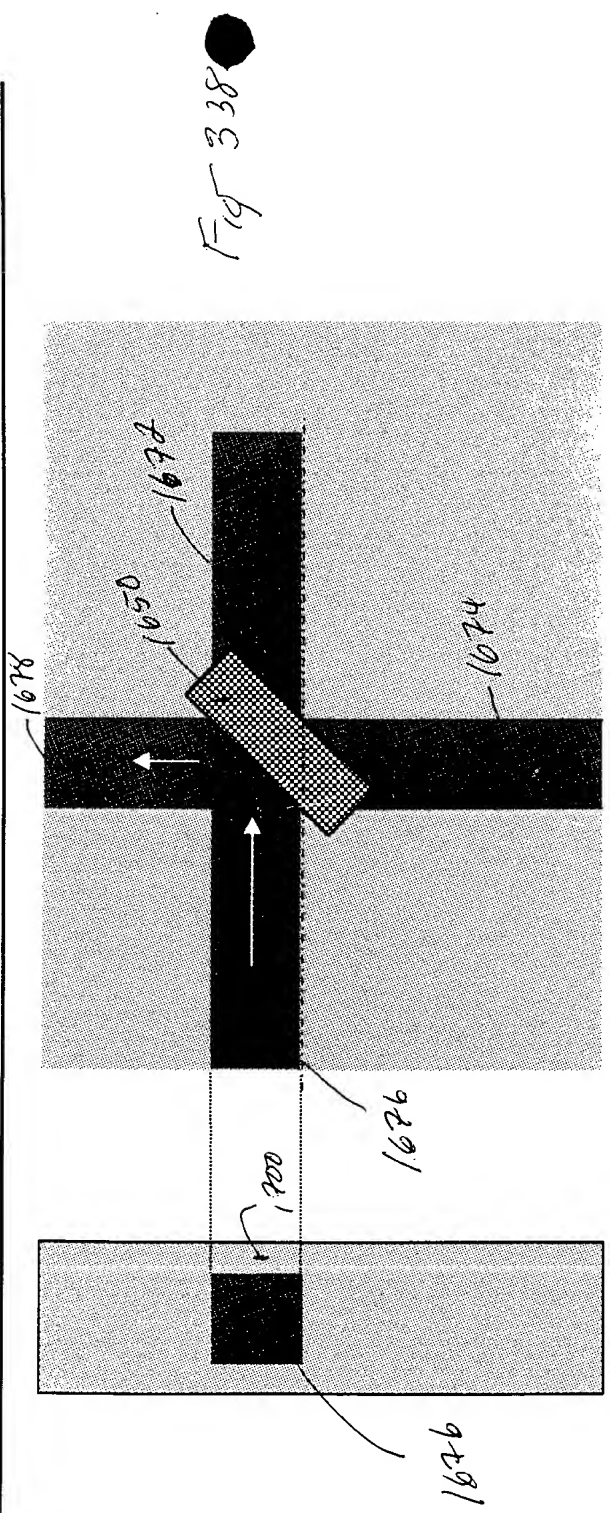


Fig. Add-9/23/99-3

# Conventional Corner Turning Structure

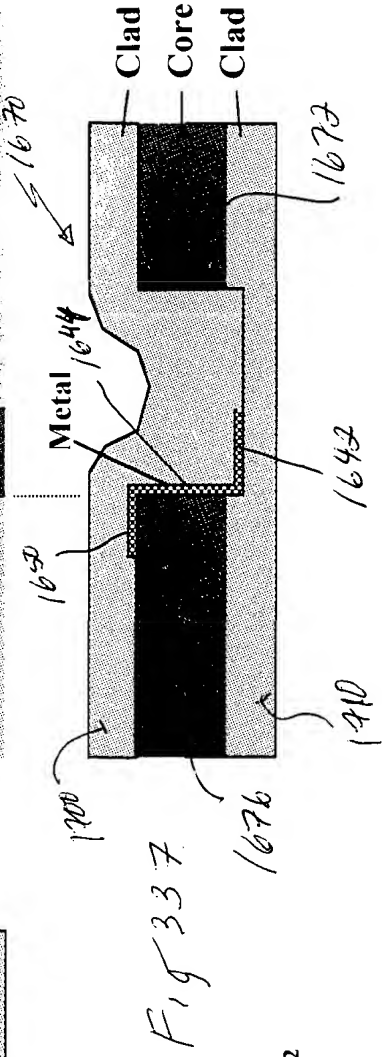
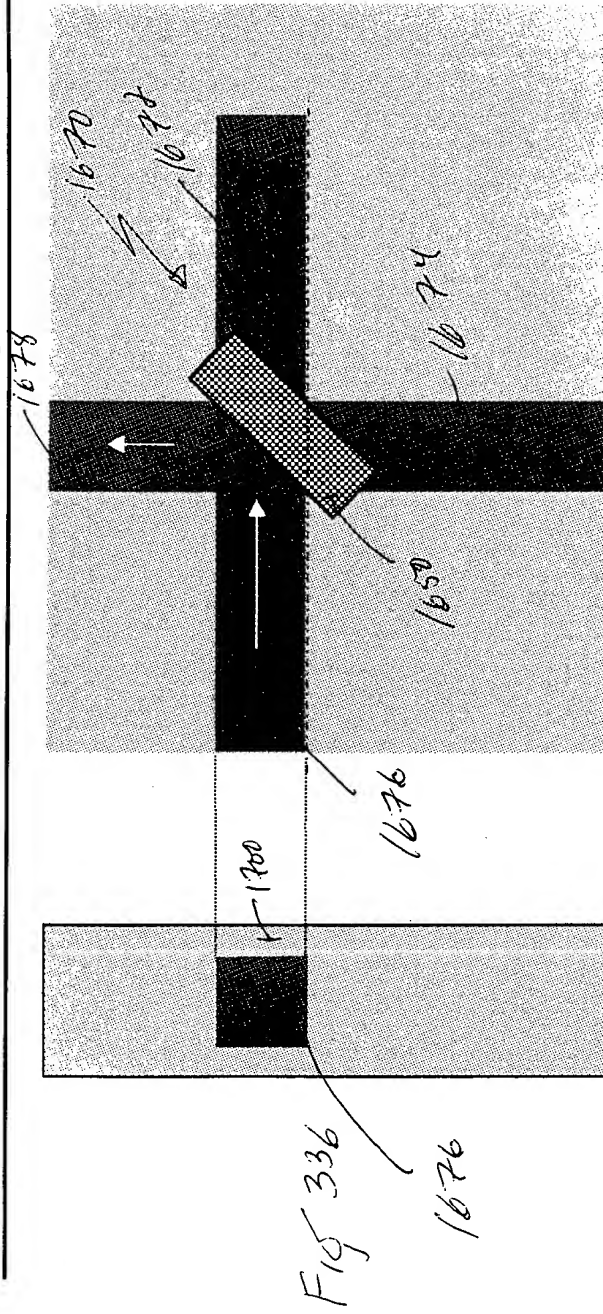
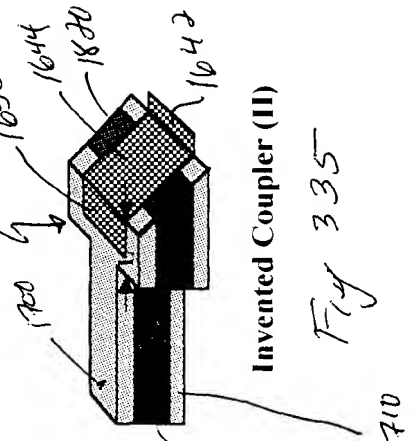
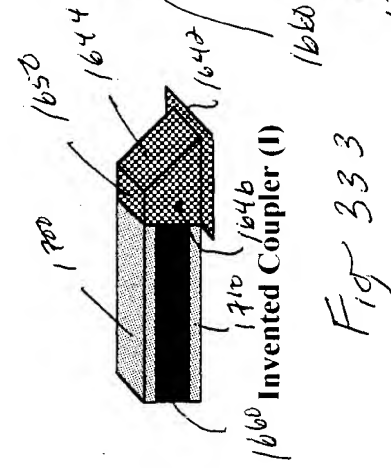
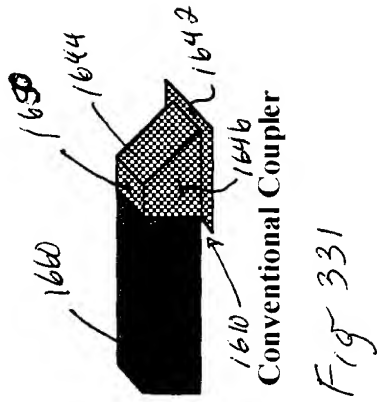
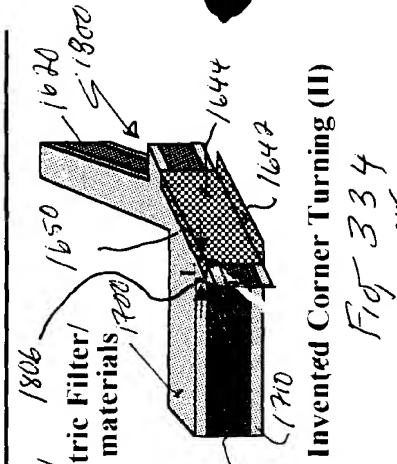
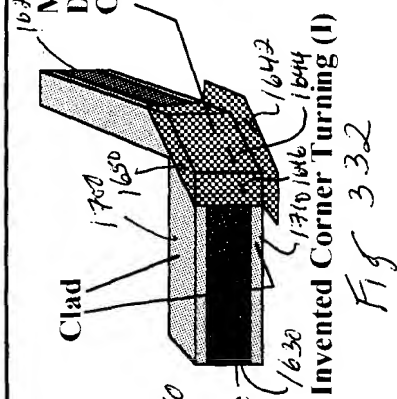
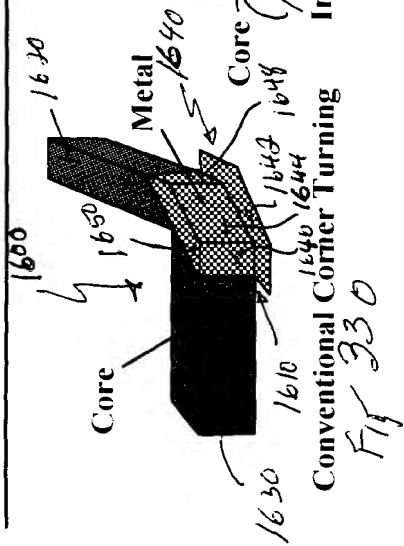


Fig. Add-9/23/99-2

# Conventional and Invented Waveguide Structure Examples



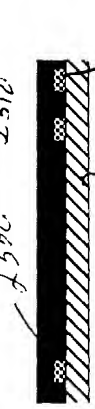
# Example 3: Z waveguide Fab. Process 1

(a1) Metal pattern formation Fig 376



(a2) Core coat9

[DuPont, AlliedSig, ORMOCERs or F-PI]

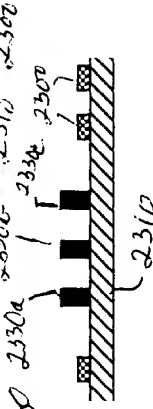


(a3) Z-WG core patterning

[UV-Exposure, mask-formation+RIE, Laser, or Dupont process]

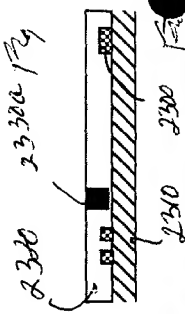
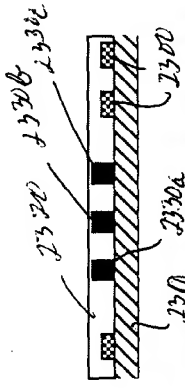
Development

(for AlliedSig, ORMOCERs)



(a4) Clad coat

(for planarization viscosity adjust if necessary CMP)



(a5) Core coat

[DuPont, AlliedSig, ORMOCERs or F-PI]

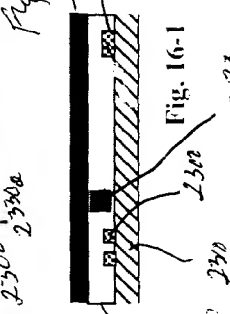
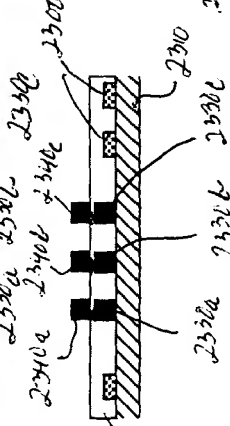


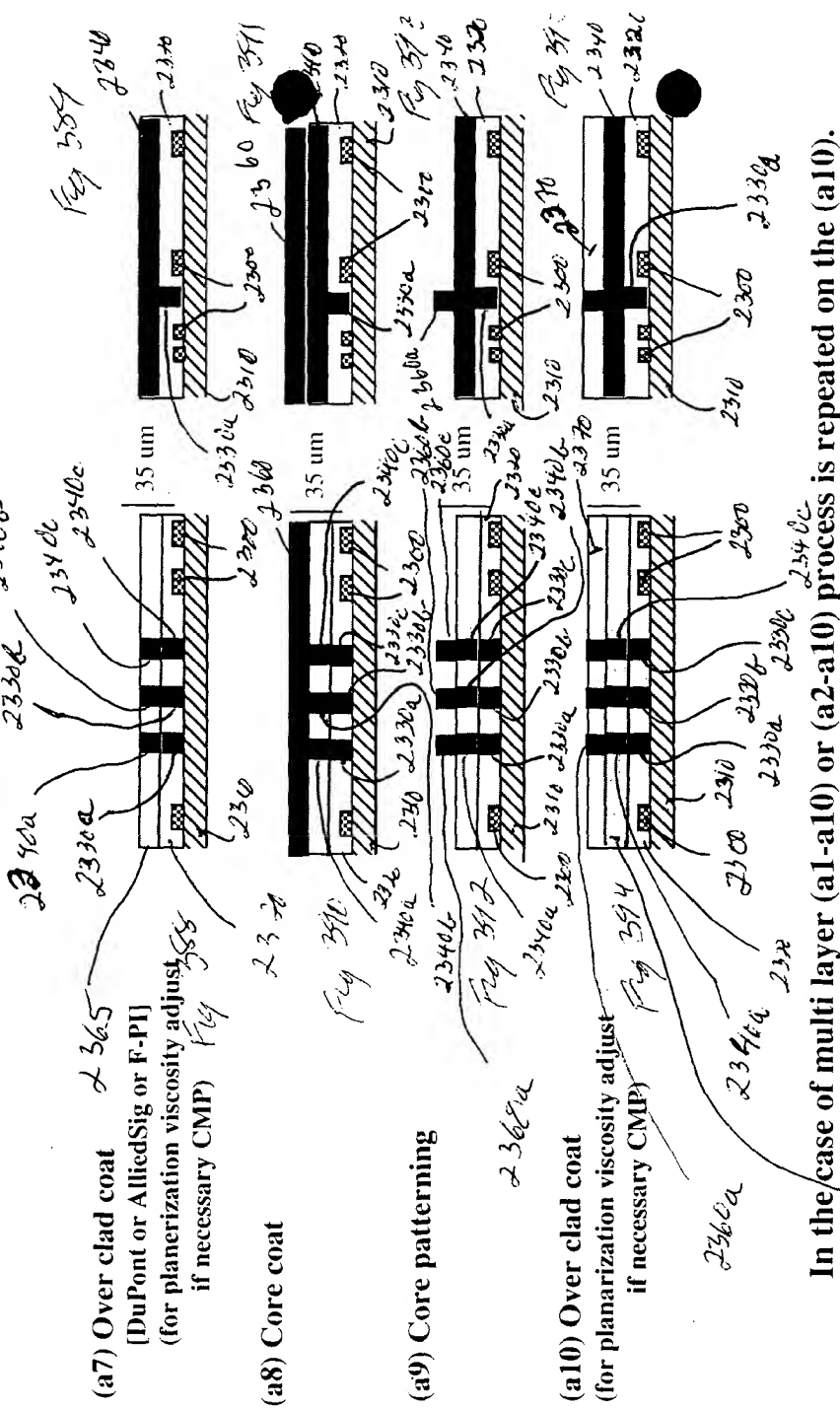
(a6) WG core patterning

[UV-Exposure, mask-formation+RIE, Laser, or Dupont process]

Development

(for AlliedSig, ORMOCERs)





**Fig. 16-2**

# Example 4: Z waveguide Fab. Process 2

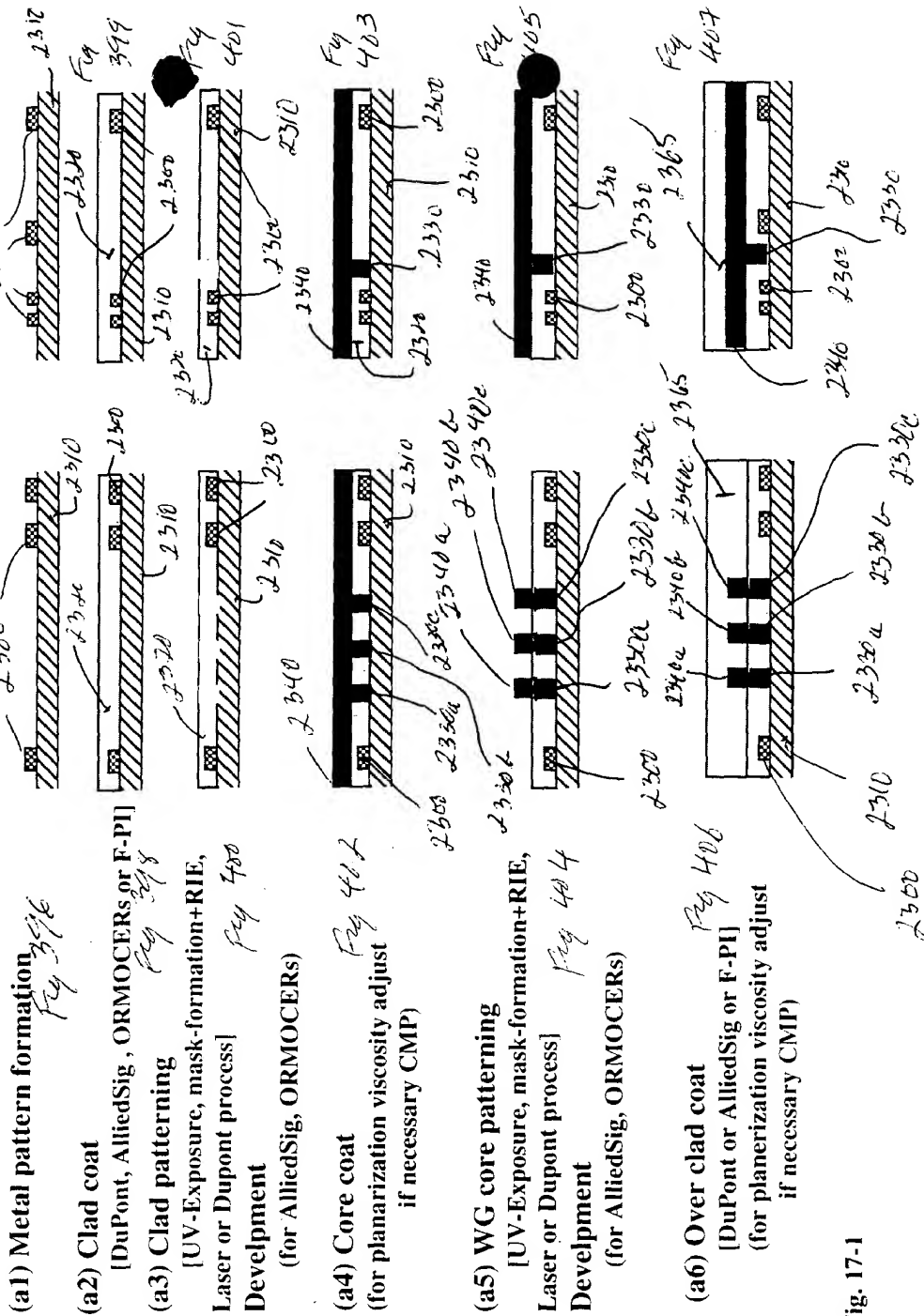
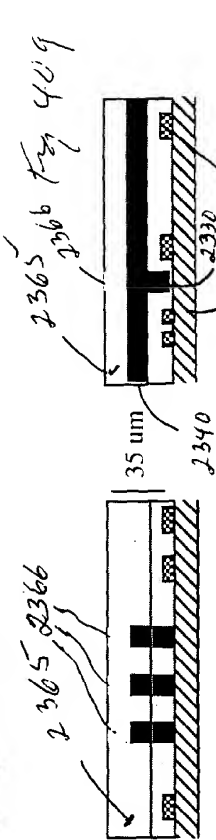


Fig. 17-1

(a7) Clad patterning

[UV-Exposure, mask-formation+RIE,  
Laser or Dupont process] Fig 408  
Development

(for AlliedSig, ORMOCERS)

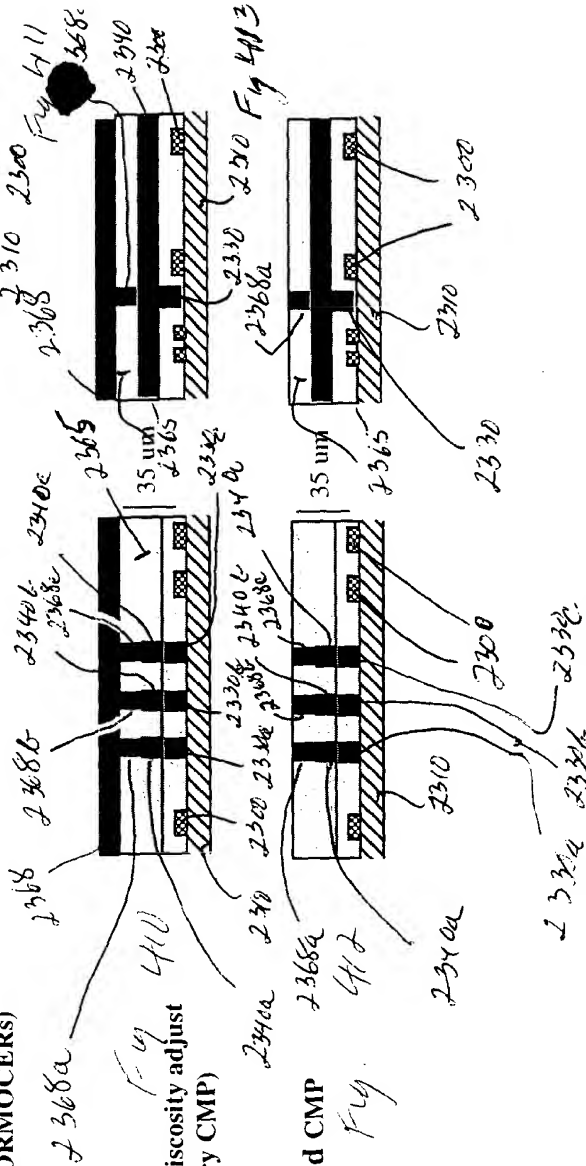


(a8) Core coat

(for planarization viscosity adjust  
if necessary CMP)

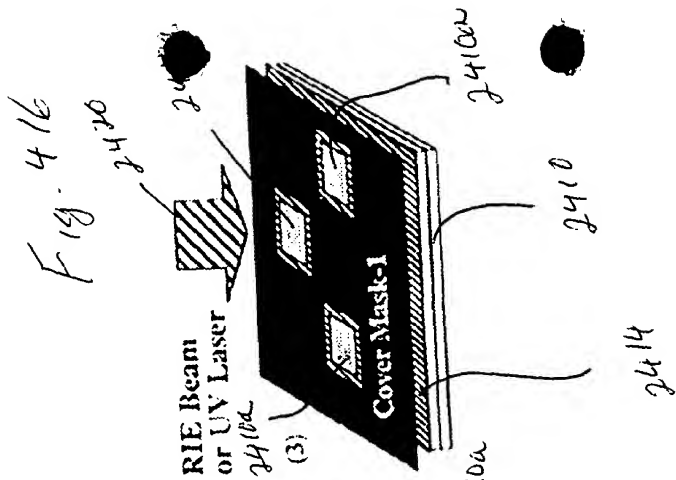
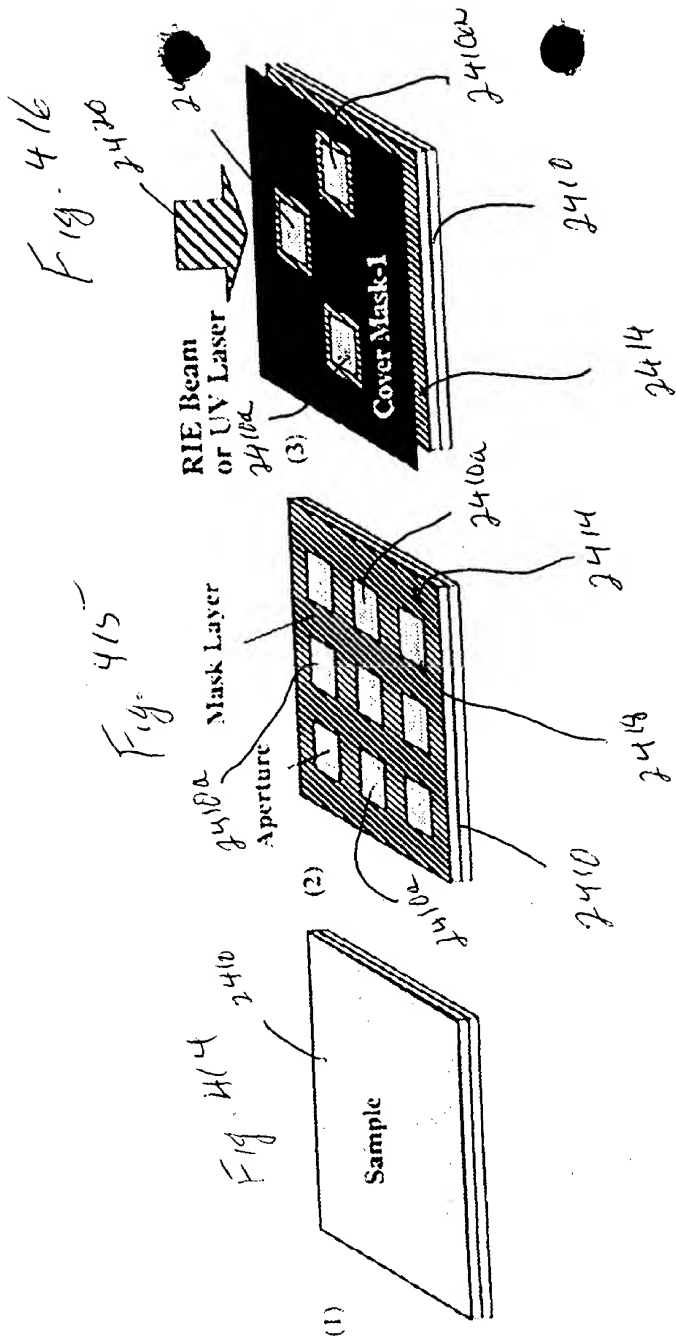
or

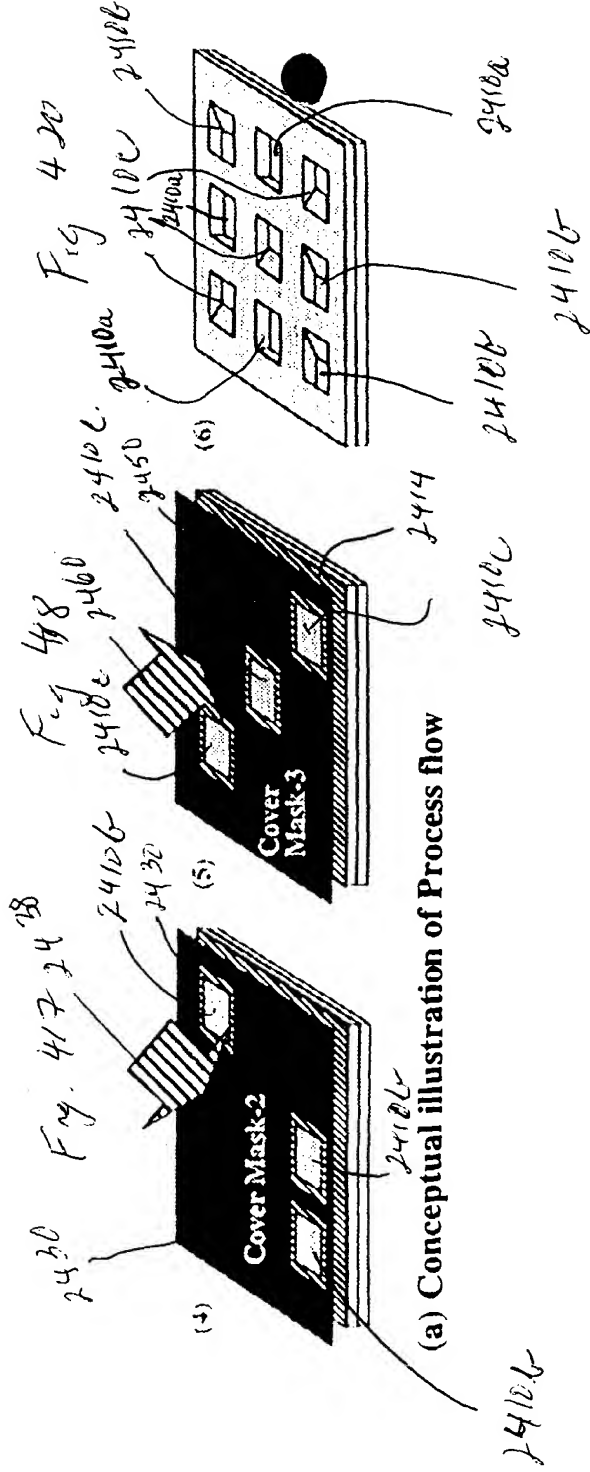
(a8) Core coat and CMP



In the case of multi layer (a1, a5-a8) or (a5-a8) process is repeated on the (a8).

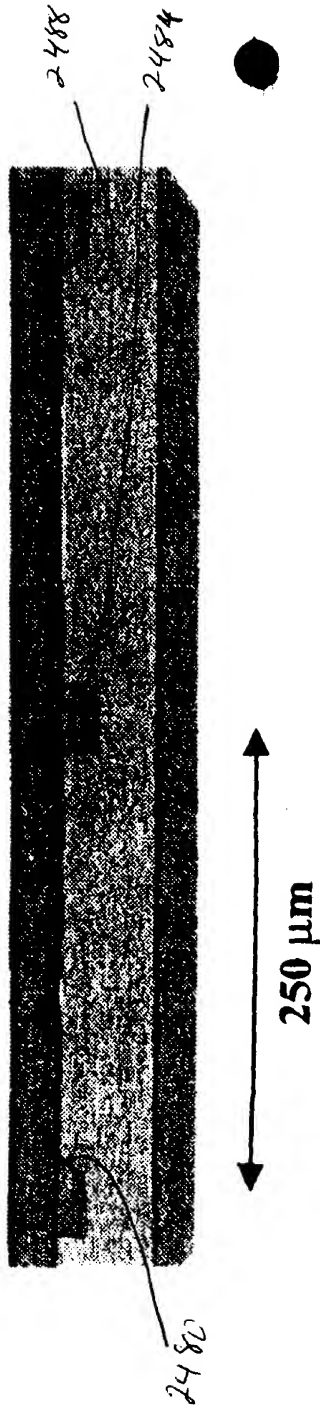






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Fig. 4d1



(b) Trench wall formation of three different angles